DC Offset Elimination in a Single Phase Grid-Connected Photovoltaic System

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ABSTRACT

Australian Standard AS 4777.2-2005, section 4.9 imposes limits on DC injection into the AC network by grid connected inverters. One way to ensure that this requirement is met is to use a power transformer as interface between the output of the inverter and the AC network. But this adds costs, mass, volume and power losses. It is, therefore, an advantage to design the inverter system so that zero DC offset is guaranteed at its output. Ideally no DC would be expected at the output of the inverter. In practice, however, in the absence of special measures, a small amount of DC is present because of circuit component imperfections. Techniques that have been proposed so far for the elimination of the DC offset current are based on the sensing of the DC offset voltage at the output of the inverter. The output of the sensor is used to drive a feedback system designed to control operation of the inverter so that the DC offset is eliminated. The focus of this paper is on the mathematical modeling of a recently proposed dc offset sensor and dc offset control system. Experimental validation of the model is presented. It is demonstrated that while satisfactory performance is achievable the technique has some serious disadvantages.

1. INTRODUCTION

Many of the dispersed generation systems that have been proposed require power electronic conversion from DC to AC. A grid connected photovoltaic (PV) system is a well-known example. DC power from the solar panels is converted to AC by an inverter before injection into the AC network. Ideally the output current of the inverter should be purely AC. But in practice it will contain a small amount of DC. Excessive DC injection into the AC network can result in problems such as corrosion in underground equipment[1], transformer saturation and transformer magnetizing current distortion[2], metering errors and malfunction of protective equipment[3]. For these reasons there are standards that impose limits on DC injection.

DC injection could be eliminated by using a power transformer as interface between the output of the inverter and the AC network. But this method has major disadvantages such as added cost, mass, volume and power losses. Alternative solutions to the DC injection problem have been proposed[1][4]. Both reference [1] and reference [4] suggest the use of a feedback loop to eliminate the DC offset. In reference [1] a simple mathematical model is developed for the feedback system. It is assumed that the inverter is voltage controlled. No experimental results are reported. Reference [4] considers a current controlled inverter. It reports some steady state performance test results. However it does not include mathematical analysis of the proposed DC offset sensor and feedback system and test results on dynamic performance are not reported.

This paper focuses on the same DC offset sensor and feedback system that has been proposed in reference [4]. An overview of the entire PV system is given in section 2 of the paper. A mathematical model for the DC offset sensor and the feedback loop is developed in section 3. Section 4 includes a discussion on important design criteria and proposes a design procedure. Comparisons between predicted and measured performance are carried out in section 5. Section 6 concludes the paper.

2. SYSTEM OVERVIEW

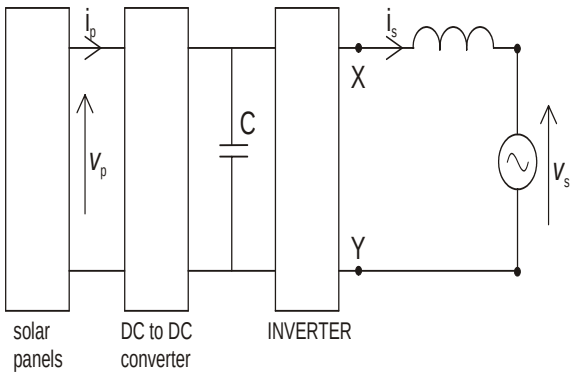


Figure 1: Grid-Connected PV System

There are a number of system configurations that have been proposed for single phase grid-connected photovoltaic (PV) systems. The configuration that has been used to evaluate the DC offset elimination method is shown in figure 1. DC voltage from the solar panels is stepped up by a DC to DC converter. The output of the DC to DC converter is connected to the DC bus whose voltage is regulated. Power from the DC bus is converted to AC by the inverter and fed into the AC network.

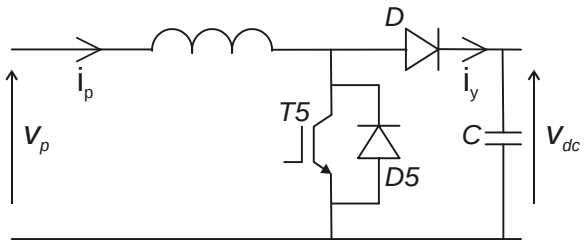


Figure 2: DC to DC Converter

The DC to DC converter, which is shown in figure 2, operates in current controlled mode. The current reference i_{pr} is determined by the maximum power tracker (figure 3). The maximum power tracking routine is invoked every few seconds. The routine is essentially a search for the value of i_{pr} that results in the maximum value of output power ($v_p i_p$) from the solar panels. Once that value is found i_{pr} is kept constant for the next few seconds. Current error i_{pe} is the difference between actual solar panel current i_p and the current reference i_{pr}. Logic within the hysteretic current controller causes transistor T5 to change state if current error i_{pe} goes outside a relatively small tolerance band centred on zero. If i_{pe} is greater than the upper limit of the tolerance band then T5 is switched on. If i_{pe} is smaller than the lower limit of the band then T5 is switched off. While i_{pe} is within the band, the state of T5 is left unchanged.

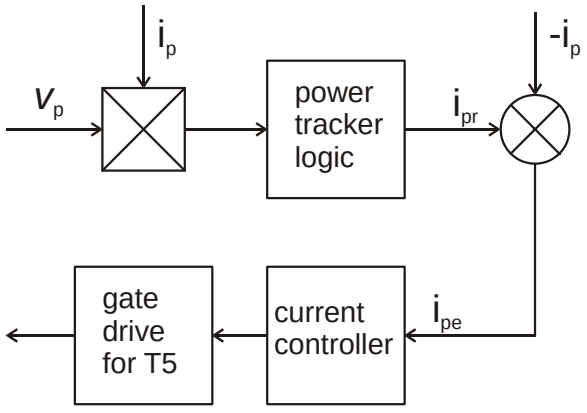
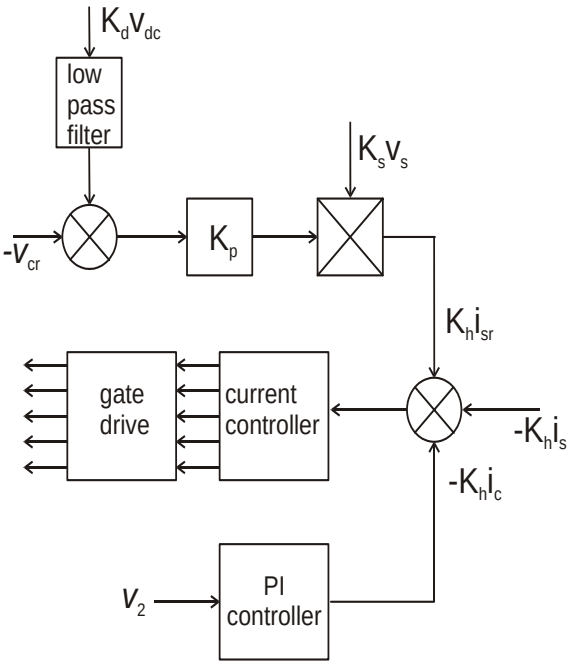


Figure 3: Block Diagram of Maximum Power Tracker



K_e =PI controller gain

τ_i =PI controller integration time

K_h = Hall effect sensor constant = 1V/A

Figure 4: Inverter Control System

The control strategy adopted for the DC bus voltage is represented in figure 4. Successful control of the DC bus voltage ensures balance between power output of the DC to DC converter and power injected into the AC network. A simple proportional controller with gain K_p is used. The DC bus voltage signal is attenuated by a factor K_d and filtered. At steady state the output of the proportional controller will be a constant value. This is multiplied by a sinusoidal signal which is in phase with the AC supply voltage v_s. The output of the multiplier, $K_h i_{sr}$, is the current reference for the inverter. A rise in output power from the solar panels will cause the DC bus voltage v_{dc} to rise. This causes the error voltage at the input of the proportional controller to rise which in turn causes the inverter current reference signal $K_h i_{sr}$ to rise. Thus the output current of the inverter goes up and more power is fed into the AC network. As expected, a rise in power output from the solar panels causes increased DC bus voltage steady state error.

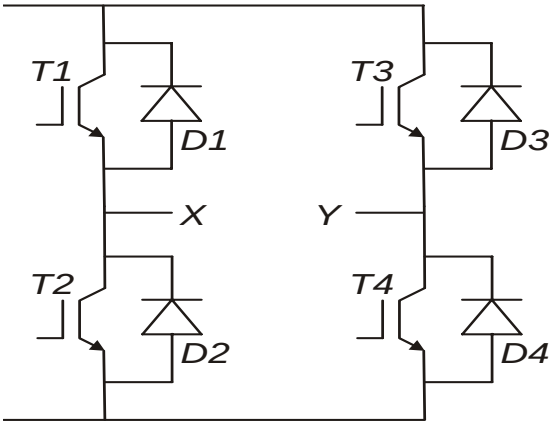
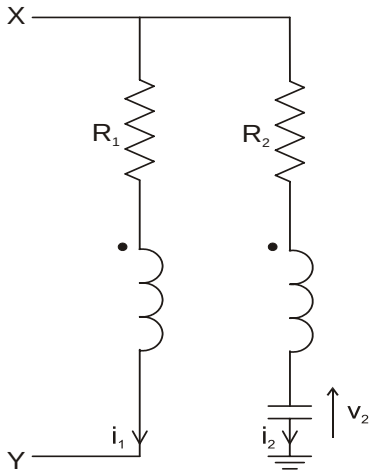


Figure 5: Inverter

Figure 4 also represents the current controller for the inverter which is shown in figure 5. The inverter is operated in unipolar mode and, since the current reference signal $K_h i_{sr}$ is in phase with voltage v_s, it operates at unity power factor. Transistor T4 is kept on (T3 kept off) throughout the duration of the positive half cycle of v_s. Similarly transistor T3 is kept on (T4 kept off) throughout the duration of the negative half cycle of v_s. The hysteretic current controller operates in such a way that current i_s tracks i_{sr}. If the DC offset compensating signal $K_h i_c$ is ignored, the current error signal is given by $K_h(i_{sr} - i_s)$. The current controller operates so as to ensure that the current error remains within a small tolerance band centred on zero. During the positive half cycle of v_s the current controller pulse width modulates T1 and T2 is kept off. Similarly during the negative half cycle of v_s the current controller pulse width modulates T2 and T1 is kept off. If, during the positive half cycle of v_s, the current error signal is greater than the upper limit of the tolerance band then T1 is switched on causing current i_s to rise because v_{dc} is always greater than $|v_s|$. If the current error signal is smaller than the lower limit of the tolerance band then T1 is switched off causing current i_s to fall. When current i_s falls, it does so through D2 under the influence of the source voltage v_s. As long as the current error signal is within the tolerance band the current controller does not change the state of T1 or T2. Operation during the negative half cycle of v_s is similar to what happens in the positive half cycle except T4, T1 and D2 respectively swap roles with T3, T2 and D1. In summary during the positive half cycle of v_s, T4 conducts continuously, T1 carries current i_s as it rises within its tolerance band and D2 carries current i_s as it falls within its the band. During the negative half cycle T3 conducts continuously, T2 carries $-i_s$ as it rises within its tolerance band and D1 carries $-i_s$ as it falls within the band. Thus current i_s closely tracks reference current i_{sr}.



L= winding inductance; M=mutual inductance=K_cL

C_2=filter capacitance; $\tau_f = R_2 C_2$

Figure 6: DC Offset Sensor

The DC offset sensor being considered is shown in figure 6 and it is based on the same concepts as those suggested in reference [4]. The 1:1 mutually coupled inductor pair is bifilar wound to minimise leakage flux. The purpose of the mutually coupled inductor pair is to minimise the 50 Hz voltage component in v_2. If R_1 and leakage flux were equal to zero then v_2 will not contain any 50 Hz component. R_1 and leakage flux are both finite and there will be some 50 Hz component in v_2. It is important to minimise that component because it interferes with operation of both the DC bus voltage controller and the inverter current controller. For example the 50 Hz part of voltage v_2 may add a quadrature component to the reference current, which if it is large enough, can cause increased distortion in current i_s since the inverter operates satisfactorily only when i_s is practically in phase with v_s.

3. MATHEMATICAL MODEL

$$\begin{pmatrix} sL+R_1 & sM & K & -K \\ sM & sL+R_2 & K+1 & -K \\ 0 & -1 & sC_2 & 0 \\ 0 & 0 & 1 & s\tau_i \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ V_2 \\ V_i \end{pmatrix} = \begin{pmatrix} V_s + I_0 R \\ V_s + I_0 R \\ 0 \\ \tau_i v(0) \end{pmatrix} \quad (1)$$

Equation 1 is a state space representation of the DC offset control system. The symbols are defined in figure 4, figure 5, in the appendix and within this section. Upper case symbols used for currents and voltages

represent the Laplace transforms of i_1, i_2, v_2, i_0, v_s and v_i. It has been assumed that the current controlled inverter is effectively a unity gain amplifier. In other words output current i_s instantaneously follows the effective current reference which is equal to $(i_{sr} - i_c)$. The voltage at the output terminals of the inverter has been approximated as $v_s + (i_0 - i_c)R$, where R is the resistance experienced by i_s as it flows from X to Y (figure 1). Current $(i_0 - i_c)$ is the offset component of current i_s. It is assumed that all the 50Hz voltage drop due to i_s is included in v_s. Since the 50Hz voltage drop due to i_s is small, a good approximation for v_s is the supply voltage. Offset current i_0 is due to circuit component imperfections. With the DC offset controller operating, a compensating current i_c is generated which, at steady state, ideally cancels i_0. The mathematical model ignores any possible interactions with other control loops in the system. Any possibility of interaction with the maximum power tracker would be through the DC bus bulk storage capacitor voltage v_{dc}. But operation of the maximum power tracker is unaffected by changes in v_{dc}. Therefore the assumption of no interaction between the DC offset controller and the maximum power tracker is justified. It can also be argued that there is very little interaction between the operation of DC offset control loop and the DC bus voltage control loop. The fundamental reason behind this is that the DC bus voltage control loop is driven by the imbalance between DC power from the DC bus and AC power injected into the AC network and that the action of the DC offset controller has practically no effect on that power balance. That is except for resistive losses, there is no active power associated with the injection of a DC offset current into the AC network. Moreover, the resistive losses are, in practice, very small. The reduction or elimination of DC offset current in i_s will therefore cause only minor reactions from the DC bus voltage control loop which will result in very slight increases in reference current i_{sr}. Thus while there is a slight effect on the DC bus voltage control loop by the DC offset controller, the latter is not affected by the former. The assumption of no interaction between the DC offset controller and the DC bus voltage control loop is therefore justified. The model represented by equation 1 can be used for both dynamic and steady state analysis. The two steady state issues that are most relevant are the steady-state behaviour of $(i_0 - i_c)$ and the 50 Hz component in v_2. Because of the integral action of the PI controller, it can be deduced that if at steady state current i_0 is constant or slowly changing then $(i_0 - i_c)$ will be zero. The 50 Hz component in v_2 gives rise to a 50 Hz component in $K_h i_c$ which must be minimised because of its adverse effect on the operation of the inverter. Equation 2 is a transfer function that has been derived from equation 1 and it can be used to evaluate the 50 Hz component of $K_h i_c$.

$$K_h I_c = \frac{K_e[\tau_p \tau_i (1-K_c)s^2 + \tau_i s + \tau_p (1-K_c)s + 1]V_s}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s^1 + b_0} \quad (2)$$

where $s = j100\pi$ rad/s

and V_s = rms value of AC supply voltage.

Aspects of dynamic performance that are of prime interest are stability and turn-on transients. At turn-on all control and gate drive circuits are energised and allowed to stabilise before inverter operation is enabled. This means that unless special measures are implemented, when the inverter starts to operate the output of the PI controller is not necessarily zero. In the worst case the PI controller output could be at its designed saturation limit. This means that turn on transients can be partly due to the initial integrator capacitor voltage $v_i(0)$. Equation 3 is a transfer function that has been derived from equation 1 and it allows the effect of $v_i(0)$ on the transient response of the compensating current to be determined.

$$K_h I_c = \frac{(f_3 s^3 + f_2 s^2 + f_1 s + 1)\tau_i K_e v_i(0)}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0} \quad (3)$$

Current i_0 will also cause a transient component in the compensating current i_c. Equation 4 allows this transient component to be determined.

$$K_h I_c = \frac{[\tau_i \tau_p (1-K_c)s^2 + \tau_i s + \tau_p (1-K_c)s + 1]K_e R I_0}{(b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + b_0)} \quad (4)$$

Stability assessment can be carried out by applying the Hurwitz criterion to the system's characteristic equation which is the denominator of equation 3 or 4. Since K_c is very close to 1, the system can be reduced to third order. Also as will be shown in the next section R_1 / R_2 is much smaller than 1. Therefore the following must be satisfied in order to guarantee stability.

$$\tau_i > \frac{\tau_f \tau_p K}{(\tau_f + \tau_p)(K+1)} \quad (5)$$

4. DC OFSET CONTROLLER DESIGN

The mathematical model presented in section 3 was used to help with the design and evaluation of a DC offset controller based on the proposed DC offset sensor. For maximum effectiveness of the mutually coupled inductor

pair, K_c must be close to 1 and τ_p must be large. Bifilar winding of the inductor pair maximises K_c. Larger values of τ_p can be achieved by using a core with large cross-sectional area and copper winding window area. If K_c is close to 1 (> 0.97), loop gain K is small and $s = j100\pi$, it can be shown by using equation 2 that:

$$K_h I_c \approx \frac{-K_e V_s}{(100\pi)^2 \tau_p \tau_f} \quad (6)$$

The following were the design steps:

(a) An available core, with cross-sectional area 50mmx30mm was used for the mutually coupled inductor pair. The core window was filled with two identical windings. The number of turns was chosen such that each can support voltage v_s without saturating the core. A value of about 0.5 second was achieved for τ_p. The winding resistance was approximately 2.0 Ω.

(b) Equation 6 was used to deduce τ_f. The PI controller gain K_e was chosen to be 1. Supply voltage V_s was taken to be 230V and a value of 10mV was used for $K_h I_c$. This was considered reasonable since, given that the Hall Effect sensor constant K_h is equal to 1V/A, the 10mV contributes to an equivalent of 10 mA of 50Hz to the inverter current controller reference. This has negligible effect on the DC bus voltage controller because the controller is designed for a rated current of 4.5A. Also the phase shift between the 10mV signal and voltage v_s is almost 180 degrees which means that the troublesome reactive component is negligible. Based on the above considerations equation 6 returned a value of 0.22 second for τ_f. A 220kΩ resistor and 2x0.47uF capacitors were used for practical realization.

(c) To ensure sufficient damping, it was decided to make τ_i equal to twice the value that results in marginal stability of the system. To come up with the desired value of τ_i, an estimate of resistance R was required. Resistance R consists of two series connected parts. One part is external to the AC network and is essentially the resistance of the current ripple filter inductor shown in figure 1. The other part is the Thevenin resistance looking back into the AC supply terminals. A value for the first part of R is easily determined. It is not easy to determine a value for the second part. However, a reasonable upper limit for that part may be arrived at from knowledge of the AC supply characteristics such as supply capacity, voltage regulation, X/R ratio and fault level. According to inequality 5, the use of an upper limit for R leads to higher values for τ_i. This is a conservative approach because a higher value of τ_i implies a more stable system. Based on the above considerations a value of 0.12 second was arrived at for τ_i.

There is some flexibility in the choice of the PI controller proportional gain K_e. However for the same sensor performance (governed by equation 6) and the same dynamic performance, lower values of K_e results in lower values of τ_i and τ_f which means smaller capacitors are needed for practical implementation. But an excessively low value of K_e may lead to implementation problems for the PI controller. A value of 0.5 was considered to be a reasonable compromise.

5. TEST RESULTS

Without the DC offset controller and with I_s equal to 1A, the measured DC offset current was 30mA. With the DC offset controller in operation, the measured DC offset current was less than 2mA. In theory this should have been zero. The non-zero value is most likely due to integrator imperfections. Figure 7 is a plot of the measured behaviour of the compensating current i_c as result of inverter turn-on. Prior to the start of inverter operation the DC offset controller was operating , but effectively in open loop. Because of that, at the start of inverter operation, the PI controller's output was saturated at the chosen limit which was set to about 0.5V. This limit represents the maximum available DC offset compensating current. There is good agreement between between the measured response of figure 7 and the theoretical response shown in figure 8 which is based on equations 3 and 4. The steady state value of the response is non-zero because a compensating signal is generated by the controller to cancel the DC offset observed on open loop. The settling time is of the order of 7 seconds. The fundamental reasons for this relatively slow response are the large values of τ_p and τ_f and the small value of loop gain K. The slow rate of response is not considered to be a serious problem because once the inverter is operational any disturbance that requires a response from the DC offset controller is unlikely to be fast changing. It was found that if the inductor connected to terminals X and Y (figure 1) is connected directly across the AC supply terminals, the settling time is greatly improved (figure 8). The reason for this is the effective cancellation of the open loop pole located at $-1/\tau_p$, which is a major reason for the slow response.

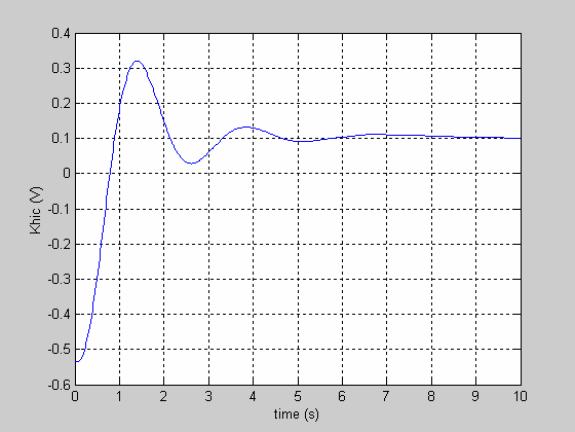


Figure 7: Measured Compensating Current Signal

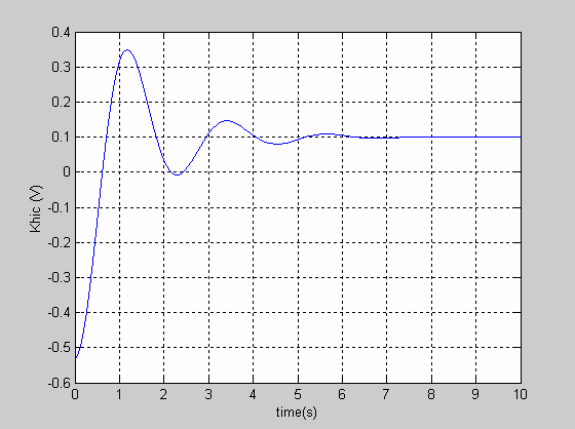


Figure 8: Predicted Compensating Current Signal

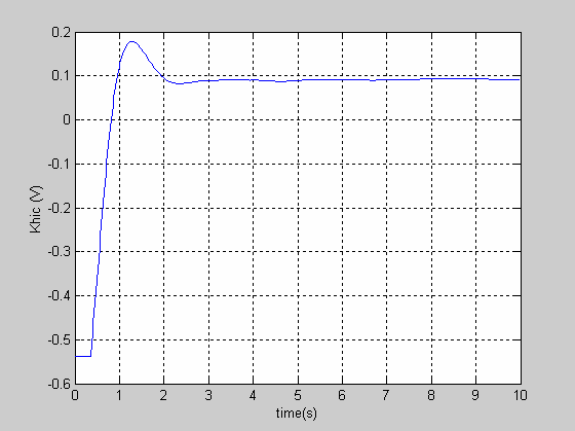


Figure 9: Measured Compensating Current Signal (one inductor directly across AC supply)

6. DISCUSSION AND CONCLUSIONS

The results presented in section 5 are considered to be very satisfactory since the DC offset controller manages to keep the DC offset well within the limits specified by Australian Standard AS 4777.2-2005. A major problem however is the size of the inductor core and the amount of copper needed by the two windings for effective filtering of the 50Hz signal. There is also significant additional power losses associated with a relatively large core. Smaller cores were not available for experimentation. But design equations for inductors show that as core area and winding window area decrease the winding resistance increases much more rapidly than its inductance. For example, for the primary side of a 230V/24V transformer with package dimensions 20x20x15mm, τ_p was measured as approximately 5ms and winding resistance was 14 kΩ. The mathematical model shows that with two such windings used as mutually coupled inductor pairs, the DC offset sensor would behave effectively as a first order filter with time constant R_2C_2. Due to the need for a large core and a significant amount of copper for the mutually coupled windings to be effective, the proposed DC offset sensor is not considered to be a practical solution to the problem of sensing the DC offset current injected by a grid-connected inverter into the AC network.

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APPENDIX

Definitions:

$$b_0 = K_e R / K_h = K$$

$$b_1 = \tau_p (1 - K_c) K + \tau_i (K + 1)$$

$$b_2 = \tau_i \tau_p (1 - K_c) K + \tau_i \tau_p + \tau_i \tau_f$$

$$b_3 = \tau_p \tau_f \tau_i (1 + R_1 / R_2)$$

$$b_4 = \tau_i \tau_f \tau_p^2 (1 - K_c^2) R_1 / R_2$$

$$f_1 = \tau_p + \tau_f ;$$

$$f_2 = \tau_p \tau_f (R_1 / R_2 + 1)$$

$$f_3 = \tau_f \tau_p^2 (1 - K_c^2) R_1 / R_2$$