UNIVERSITY OF SOUTHERN QUEENSLAND

SINGLE-PHASE TRANSFORMERLESS UNIPOLAR SWITCHED INVERTERS FOR UTILITY-CONNECTED PHOTOVOLTAIC APPLICATIONS

A dissertation submitted by

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ABSTRACT

The disadvantages of using solar energy are its capital cost (which is about A$6/W), in comparison to that of conventional sources of energy (which is about A$1.80/W), and its conversion efficiency, which in commercially available Photovoltaic (PV) systems is less than 20%. Consequently, for utility connected PV generation to become a viable alternative energy source, its efficiency needs to be improved, its cost reduced, and the quality of power supplied by the inverters must meet stringent standards.

This dissertation describes the research work carried out to optimise the conversion efficiency and to minimise the cost of a single-phase, hysteretic current control unipolar switched inverter system, for use as an interface between solar panels and the grid network. The 1 kW (peak power) PV system being considered does not use energy storage batteries and the inverter output is connected to the grid supply without the use of a power transformer. Improvements in the efficiency of such an inverter system often come at the expense of the quality of its output power and an increase in cost. However, in the proposed inverter system the harmonics of the output current has been improved without compromising its overall efficiency or its cost. An improvement in power quality has been achieved using a novel AC split-inductor filter network that reduces electromagnetic interference, prevents unwanted operation of the inverter switches, attenuates switching frequency harmonics, minimises low frequency harmonics and provides an average value of the inverter output current necessary for the removal of DC offset currents.

An improvement in inverter efficiency and a reduction in cost has been achieved by omitting the 50 Hz power transformer (transformerless) and by optimising the inverter current control strategies. In Australia, some power supply authorities permit transformerless PV inverters of less than 10 kW rating to be connected to their supply system. However, avoiding the use of transformers can lead to magnitudes of DC offset current outside the limits specified by Australian Standard 4777.2, 2005 being injected into the grid supply. In this project a new cost effective DC offset current

controller that removes DC offset current from the output of the inverter has been realised. This result translates into two primary benefits; firstly, a saving of about 20% in the cost of the power transformer and in the cost of providing additional solar panels to overcome transformer power losses, and secondly the DC offset controller can also be utilised in inverter applications where power transformers are used, to prevent distortion of the magnetising current.

The novel design procedure proposed in this thesis for a current controller takes into account intentional and unintentional switching circuit delays, and yields higher efficiencies without sacrificing power quality or increasing the cost of the inverter system. The inclusion of the effect of circuit delays in the design procedure is significant as it is shown that delay not only has an adverse effect on the performance of the current controller but also on the efficiency and the power quality of the inverter system.

Of paramount importance for the successful completion of this project was the relationship between switching circuit delays and the level of low frequency harmonics generated by unipolar switched inverters. Theoretical analysis is developed to show why circuit delays, inverter DC input voltage and the inductance of the current loop, are responsible for low frequency harmonics in unipolar switched and not in bipolar switched inverters. It has also been established that unipolar switched inverters can be designed to operate within the limits specified by the Australian Standard 4777.2, 2005 and that the low frequency harmonics can be maintained at acceptable levels.

For a current controller using unipolar switching, the choice of only one of four equivalent switching combinations of the inverter switches leads to suppression of switching noise, and prevents unwanted switching without the need for additional filters. Results are presented to demonstrate the unique advantage of unipolar switching over bipolar switching.

CERTIFICATION OF DISSERTATION

I certify that the ideas, experimental work, results, analyses, software and conclusions reported in this dissertation are entirely my own effort, except where otherwise acknowledged. I also certify that the work is original and has not been previously submitted for any other award, except where otherwise acknowledged.

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Signature of Candidate Date

ENDORSEMENT

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Signature of Supervisor Date

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Signature of Supervisor Date

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CONTENTS

Page

CHAPTER 3: CURRENT LOOP: UNIPOLAR VERSUS BIPOLAR SWITCHING

CHAPTER 4: CURRENT LOOP: DESIGN AND TESTING

CHAPTER 5: SWITCHING FREQUENCY FILTER DESIGN

CHAPTER 6: VOLTAGE LOOP: P-CONTROLLER VERSUS PI-CONTROLLER

CHAPTER 7: VOLTAGE LOOP: DESIGN AND TESTING

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

CCL	Current Control Loop
DCOC	DC Offset Current
EMC	Electromagnetic Compatibility
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PCC	Point of Common Coupling
PV	Photovoltaic
PWM	Pulse Width Modulation
RFI	Radio Frequency Interference
SFF	Switching Frequency Filter
THD	Total Harmonic Distortion
UTS	Utility Tie System
UPS	Uninterruptible Power Supplies
VCL	Voltage Control Loop

SYMBOLIC CONVENTIONS

The convention for symbols used for instantaneous values of variables such as voltages, current, and power, is that they are denoted by lowercase letters *v*, *i* and *p* respectively. These instantaneous quantities are a function of time but are shown for example as *i* rather then explicitly as *i* (t).

The symbols for the root mean square (rms) values of AC quantities and the average value of DC and power quantities are denoted by uppercase letters. For an example, *V*, *I* denote rms values of AC voltages and currents. The peak values of AC quantities are indicated by a symbol above the uppercase letter eg $\hat{V}$.

LIST OF PRINCIPLE SYMBOLS

C	DC input capacitor
i_p	Output current from Solar panels
i_{pref}	Reference current output from the maximum power point tracker
i_y	Output current from the DC to DC converter
i_s	Inverter output current injected into the grid supply
i_{sref}	Reference AC current
i_u	Upper tolerance band current limit
i_L	Lower tolerance band current limit
I_{Tol}	Magnitude of the tolerance band current
I_{AV}	Average inverter AC output current
K_p	Voltage controller gain
L	Inverter current loop inductance
L_s	AC source inductance
V_c	Inverter DC input voltage
V_{cref}	DC reference voltage
V_e	DC input voltage error
V_{fa}	Attenuated 100 Hz ripple free inverter input DC voltage
v_P	Solar panel DC voltage
V_s	DC supply voltage
V_{fs}	Attenuated and filtered AC supply voltage
V_{ref}	DC reference voltage from maximum power point tracker
τ_{fc}	Time constant of filter to remove 100 Hz ripple from DC voltage
τ_{fa}	Time constant of filter to remove noise from AC supply voltage
t_d	Switching circuit delay
t_r	Current rise time
t_f	Current fall time

CHAPTER 1

INTRODUCTION

1.1 Background

The importance of renewable energy sources is recognised by both the general public and the power industries. Some researchers believe the concern for environmental damage is now an even greater priority than the need to preserve the finite natural resources for future generations [1].

In Australia, the electricity industry has been restructured into four sectors namely- generation, high voltage transmission, distribution and retail supply. The benefits of restructuring are:-

- competition created in the electricity generation industry and
- the ability of individual customers to choose the most economical retailer to supply power to them.

This choice is important as surveys in the United States of electricity consumers show that up to 70% are willing to pay a premium on electricity bills to support the development of renewable energy sources [2]. Surveys of urban and rural electricity consumers in Australia also show that 67% are willing to pay a premium on electricity bills [2] for similar reasons. This significant public support provided excellent impetus to design a technically proven low cost alternative to electricity produced by using fossil fuel. Photovoltaic (PV) generation is one such alternative although at present it is not an economical method of producing electrical energy except in special, usually remote, applications.

The increase in the number of Australian electricity authorities in search of sustainable energy sources further proves the importance given to renewable energy. Many of these electricity authorities are evaluating grid-connected PV systems as an alternative source of electricity.

Grid-connected PV systems, when located at the point of use have potential benefits such as reduction in:-

- transmission power losses,
- transmission line capacity requirement,
- conventional generation capacity requirement,
- CO_2 emissions and fuel costs.

These benefits are maximised in parts of Australia and other tropical countries where the peak insolation level (sunlight intensity) coincides with peak load demand.

The amount of electrical energy produced by a PV system connected to a consumer does not always coincide with the energy demand of that consumer. Therefore, to use all the energy produced from such a system requires large energy storage capacity to be used in conjunction with the PV generation. Alternatively, a more economical method would be to directly feed any excess energy from the PV system to the grid network. The advantage of utility connected PV generation over the stand-alone systems is that back-up generation and bulk storage are shared.

In the utility interactive PV system being considered, utility back-up ability is required. Such a system, also referred to as the *Utility Tie System* (UTS), allows direct conversion of PV energy to utility power without using storage batteries. In domestic applications the advantages of avoiding the use of batteries for storage of surplus energy from the PV panels are:-

- reduced capital and maintenance cost of the PV system

- removal of all health and safety problems associated with batteries from consumers premises

However, without storage batteries, the fluctuating DC power produced by the solar panels, as a result of variations in insolation level, has to be converted into a sinusoidal output of acceptable quality by an inverter, and then supplied to the grid. Although the inverter described in this project is specifically for grid-connected PV systems, it can be used for other traditional applications such as in uninterruptible power supplies (UPS), motor controls and voltage regulation systems.

The main disadvantages of using PV energy are its capital cost (about A$6/W) in comparison to that of the conventional sources of energy (about A$1.80/W) and its conversion efficiency, which in commercially available PV systems is less than 20%. Consequently, for utility connected PV generation to become a viable alternative energy source not only must the cost of the PV panels and the inverter system be reduced but also its efficiency needs to be improved.

In Australia, research to produce PV panels that are more efficient is being undertaken by other institutions (e.g. University of New South Wales) and therefore was outside the scope of this project. The main focus of this project was to improve the conversion efficiency of the inverter equipment, which acts as an interface between the PV panels and the grid network. Higher efficiencies were to be achieved with improved quality of inverter output power and with reduced cost.

Inverters are being used in domestic systems in Australia. The capacity of a distributed residential system would typically be less than 5 kW. The Solar Olympic Village in Sydney, which comprises 665 permanent homes with 1 kW PV systems connected to the grid via inverters, is an example of such a system. In this Sydney project however, transformers are used between the inverter output and the grid system. Therefore, injection of unwanted DC offset current into the grid network was not an issue. In the proposed project however, one of the methods used to reduce power loss, cost and size of the inverter system was to avoid the use of 50 Hz power

transformers (transformerless) and therefore the magnitude of DC offset current injected into the grid is a critical issue.

Some electricity authorities in Australia permit the connection of transformerless inverter systems directly to their grid network provided that they are of less than 10 kW rating. However, the method of controlling the magnitude of DC offset current injected into the grid system ultimately determines if the use of transformers could be avoided. In Australia, for PV inverters to be directly connected to the grid, DC current injection should not exceed 5 mA or 0.5 % of the rated output current whichever is greater [3, 4]. An exhaustive literature review revealed that there were no published data available for typical values of DC offset current generated by single phase transformerless PV inverters. There was also no published evidence that the DC offset current from transformerless inverters could be economically maintained below the acceptable limits without compromising the efficiency and the quality of the inverter output power. Therefore, to achieve the aims of this project there was a need to develop a new control technique to remove DC offset current generated.

A second method of optimising the efficiency of PV inverters that was considered was the use of unipolar switched inverters for utility connected application. An advantage of using unipolar switching was that it led to lower power losses. However, there was no evidence that the magnitude of switching frequency current harmonics generated by unipolar switched inverters will be within the limits specified by the Australian standard 4777.2, 2005 [4]. This issue had not been previously investigated and was of paramount importance in the proposed utility connected PV applications.

There was also a need to develop current controller design procedures that lead to optimum inverter efficiencies. However, these desired higher efficiencies could only be realised if: -

- the output from the inverter system met the requirements set by Australian Standards [4] and the local electrical supply authority
- they were achieved without an increase in the cost of the inverter system

- the safety and reliability of the conventional supply system was not compromised.

It was envisaged that the improvement of efficiency will lead to the following: -

- less copper required for the output filter inductor;
- reduction in the switching losses and hence size of the heat sinks required;
- reduction in the overall physical size and cost of the inverter;
- removal of inverter fixed losses

However, it is also apparent that reducing the resistance of the current loop to improve inverter efficiency may introduce stability problems when the inverter system is subjected to disturbances caused by switching events. Therefore, when designing inverters for a grid connected PV system it is essential to establish the relationship between: -

- efficiency and stability
- efficiency and inverter power quality

A practical inverter system cannot be constructed without implementation delays. Implementation delays consist of intentional delays such as blanking or dead times and unintentional delays such as circuit propagation delays. Based on an extensive literature review, there was no evidence of any published design procedure specifically for transformerless unipolar switched inverters for PV grid applications that included the effect of implementation delays when determining: -

a) the minimum value of the inductance of the inverter current control loop required to achieve maximum efficiencies while maintaining current harmonics injected into the grid system at acceptable levels
b) the minimum inverter input DC voltage consistent with minimising switching loss
c) the level of switching frequency current harmonics injected into the grid supply

d) the performance of AC filter networks

The above issues related to implementation delay are all critical to the success of this project and will need to be analysed.

Utility connected PV inverters and other sensitive electrical equipment are likely to be connected to a *point of common coupling* (PCC). Therefore the switching frequency harmonics generated by these inverters may cause malfunction of such sensitive equipment. To avoid harmonic related problems, AC filters need to be designed to keep the level of switching frequency current harmonics being injected into the grid system within the limits specified by Australian standard 4777.2, 2005 [4]. There is no evidence that such AC filters can be designed without compromising the overall efficiency and the performance of the unipolar switched inverter systems. The level of switching frequency harmonics generated by unipolar switched inverters, and techniques to attenuate these harmonics (without increase in inverter power losses), will be fully investigated in this project.

The large number of control loops (and variables) that need to be considered to achieve higher efficiencies without sacrificing the inverter power quality (and cost), and the constraints imposed by the Australian Standards [3, 4], makes this project challenging. The list of strategies, likely problems and the possible solutions to be investigated to achieve higher inverter efficiencies, lower cost, and improved power quality are summarised in Table 1.1.

Strategies to Achieve Maximum Efficiency	Adverse Effects on Power Quality	Nature of Solutions to be Investigated
1) Transformerless Operation	Risk of unacceptable levels of offset DC current injection into the grid system	Development of cost effective techniques to remove DC offset current
	Increased risk of Electromagnetic Compatibility problems	Options for designing current and voltage controllers which minimise EMC problems
2) Unipolar Switching	Possible problems with:- a) current distortion at zero crossing b) unacceptable levels of low frequency and switching frequency harmonics injected into the grid system	Exploring the use of:- a) current steering AC filter designs to remove current harmonics b) feedback loop designs to minimise low frequency harmonics.

Table 1.1: Summary of strategies to maximise inverter efficiencies

1.2. Project Objectives

The main aim of this project was to develop a new design procedure for a single-phase, transformerless PV inverter system suitable for grid connection, which would lead to higher inverter efficiencies, improved output power quality and reduced cost. Detailed performance analyses of both the unipolar and the bipolar switched inverters will be carried out before a final choice is made.

Techniques to remove DC offset current will be investigated to ensure that the DC current injected into the grid system is maintained within the legal limits irrespective of its source. To improve the quality of inverter output current, a suitable efficient and cost effective ripple current filter design will also be developed.

The specific objectives of the project are summarised as: -

(a) to confirm that interactions between the voltage control loop, current control loop and DC control loops are weak enough to be neglected and hence each loop can be designed separately;

(b) to define relevant performance criteria and develop design procedures for the voltage and current control loops that would yield component values of these two control loops such that optimum efficiency is achieved without compromising power quality;

(c) to develop a SIMULINK model of the voltage and current loops and use the control loop parameters obtained in (b) to determine the theoretical performance characteristics of the inverter system;

(d) to construct and test the inverter control loops based on the design process developed in (c);

(e) to design and test a ripple current filter that does not compromise the efficiency of the inverter system and is in compliances with section 4.5, AS4777.2, 2005;

(f) to design and test a DC current controller that ensures that the DC offset current present at the output of the inverter is in compliances with section 4.9, AS4777.2, 2005 and hence makes it possible to avoid the use of power transformers;

(g) to obtain experimental results to validate that higher efficiencies of the proposed inverter system can be achieved without compromising the quality of output power fed to the grid system or its cost.

1.3. Outline of Dissertation

The main focus of the work carried out in this project was to improve the efficiency of a PV inverter system without compromising the quality of power supplied and with reduced cost. The design procedures, the circuit construction and the testing of the current control loop (main source of power loss), is presented in Chapters 3 and 4. The switching frequency filter, the voltage control loop and the DC offset current controller are dealt with in Chapters 5 to 8. The final chapter is a review of the project outcomes. An overview of each chapter is as follows:-

Chapter 2.0 – Review of Utility Connected PV Systems

A background of the utility connected PV system is presented in Chapter 2. It includes a review of current theory, design and practices that are related to areas such as battery energy storage systems, maximum power point tracking, DC to DC converters, grid connected PV systems, inverter designs, reversible rectifiers, switch-mode power factor controllers, power quality issues, the effects and methods of control of DC offset current injection into grid supply, and finally ripple current filtering.

Chapter 3 - Current Loop: Unipolar Versus Bipolar Switching

In Chapter 3, mathematical and SIMULINK models of the current control loop using both unipolar and bipolar switching are developed. Simulation results of the effect of delay on the performance of the current loop using both unipolar and bipolar switching are also presented here.

Chapter 4 - Current Loop: Design and Testing

Chapter 4 provides a brief description of the circuits used to implement the design procedure of the current control loop developed in Chapter 3. Experimental results showing the effect of delay on the performance of the current controller are also presented in this chapter.

Chapter 5 - Switching Frequency Filter Design

Chapter 5 includes the design procedure of a simple, cost effective, negligible loss, switching frequency filter. Theoretical and experimental results are presented to confirm that the filter performed satisfactorily.

Chapter 6 - Voltage Loop: P-Controller versus PI-Controller

Chapter 6 describes the mathematical models and computer simulations of the voltage control loop using SIMULINK. These are essentially large signal models with the non-linearities of components such as multipliers (used in controller circuits) ignored. Theoretical results to confirm that interactions between the voltage and current loops are insignificant are also presented in this chapter.

Chapter 7 - Voltage Loop: Design and Testing

A brief description of the circuits developed to implement the inverter voltage control loop designed in Chapter 6 is outlined in Chapter 7. Experimental results presented in this chapter confirm that the voltage control loop can be designed separately.

Chapter 8 - Removal of DC Offset Current

The process of controlling the magnitude of DC offset current injected into the grid system is presented in Chapter 8. A new technique to remove small magnitudes of DC offset current from large values of AC current at the inverter output is presented in this chapter.

Chapter 9 - Discussions and Conclusions

A brief summary of important outcomes and suggestions for further work are outlined in chapter 9.

1.4. Summary of Original Contributions

In the process of implementing the objectives of this project, original design procedures and control techniques have been derived in areas related to the inverter control loops, AC filter network and DC current controller. These original contributions are summarised as follows: -

A) A new systematic design procedure of the inverter current control loop using unipolar switching has been developed. The procedure allows the determination of the current loop parameters; inductance value (L), magnitude of inverter input DC voltage (V_c), magnitude of tolerance band (I_{Tol}) and the maximum circuit delay (t_d) that can be tolerated if a given range of switching frequencies is to be achieved. The new equations developed in this design process allow designers to estimate not only the switching frequencies along the current waveform but also to determine three key frequencies of interest when the unipolar mode is used. These are:

- the minimum switching frequency which occurs when the inverter output current I_s is zero ($\theta = 0^o$) is:

$$F_{min} = \frac{L\ \omega \hat{I}_s}{L\ I_{Tol} + V_c\ t_d}$$

- the switching frequency when the current I_s is at its peak ($\theta = 90^o$):

$$F_{med} = \frac{\hat{V}_s(V_c - \hat{V}_s)}{V_c(L\ I_{Tol} + V_c t_d)}$$ where V_s is the AC mains supply voltage

- the maximum switching frequency, found by equating the derivative of the switching frequencies with respect to angle θ to zero, and is equal to:

$$F_{max} = \frac{V_c}{4(L\ I_{Tol} + V_c t_d)}$$

Experimental results have been presented to validate the theoretical design procedure.

While the review of literature carried out in Chapter 2 revealed that the design of bipolar inverters with circuit delays was developed by others, the outputs from these inverters were not for direct connection to the grid supply. Therefore, new equations and SIMULINK models were also developed for bipolar switched inverters to identify current loop parameters that influenced key switching frequencies and generation of low frequency harmonics. These are:-

- the minimum switching frequency which occurs when the inverter output current I_s is at its peak value ($\theta = 90^o$) is:

$$F_{min} \approx \frac{(V_c^2 - \hat{V}_s^2)}{2V_c(L\,I_{Tol} + 2V_c t_d)}$$

- the maximum switching frequency which occurs when the inverter output current I_s is zero ($\theta = 0^o$) is:

$$F_{max} \approx \frac{V_c}{2(LI_{tol} + 2V_c t_d)}$$

These equations also allowed for detailed analyses of both bipolar and unipolar switched inverters in terms of switching frequencies and switching frequencies harmonics to be carried out in this project.

B) It is shown in this project that the condition for the hysteretic or tolerance band technique to successfully control the switching frequency of the inverter switches is:

$$t_d < \frac{I_{Tol} L}{V_c}.$$

If this condition is not met then the tolerance band I_{Tol} will not be able to control the magnitude of the ripple current and limit cycle may exist.

C) The use of unipolar control leads to lower switching losses and lower filter inductor power losses. This has been identified by other researchers, as reviewed in Chapter 2. However in all these cases, the effects of implementation delay (t_d) on the level of current harmonics present in the inverter output were ignored. New mathematical and SIMULINK models have been developed in this project to show that switching delays can lead to the generation of unacceptable levels of low

frequency current harmonics. New equations to determine the average value (I_{av}) of the inverter output current have been developed to explain why only unipolar switched inverters generate low frequency harmonics. A summary of the reasons is:

- The average value I_{av} is always lower than the reference current I_{ref} near their peak values by a factor of $\left(-\frac{t_d\hat{V}_s}{L}\right)$. This reduction factor is applicable to both the unipolar and the bipolar switched inverters. However, this term is not responsible for the generation of low frequency harmonics.

- Distortion of I_{av}, signifying the presence of low frequency harmonics, is due to a component of I_{av} that is approximately a square wave, with amplitude equal to $\left(\frac{t_d V_c}{2L}\right)$. This square wave component contributes to all the odd harmonics, which are:

$$I_{s_n} \approx \left(\frac{t_d V_c}{2L}\right)\frac{4}{n\pi} \quad \text{where n is an odd number.}$$

This square wave term $\left(\frac{t_d V_c}{2L}\right)$ is not in the equation to determine the average current for bipolar switched inverters. Hence bipolar switched inverters do not generate low frequency harmonics.

Consequently switching circuit delays cannot be ignored in unipolar switched inverter design procedures.

D) Unipolar switching allows the user to choose from four theoretically equivalent methods of switching the inverter electronic switches. However, in this project it has been shown that only one of these four options results in the suppression of internal switching noise, and avoids the need for additional filtering of the feedback current to prevent unwanted switching.

E) The design of a novel AC split inductor filter network that reduces EMI generation, prevents unwanted operation of the inverter switches, removes switching frequency harmonics, attenuates low frequency harmonics and provides an average current essential for the removal of the DC offset current. It is shown that attenuation of these current harmonics can be achieved without sacrificing the overall conversion

efficiency of the inverter. Simulation and experimental results are presented to confirm that the split inductor AC filter arrangement not only removes the ripple from the output current without any adverse affects but is also a very cost effective method to use.

F) A novel control technique to remove the DC offset current from the output of a transformerless PV inverter for utility connection has been realised. Experimental results are presented to confirm that provided the inductance of the current loop is small, zero DC offset current can be maintained irrespective of the source of the DC offset current. The new DC offset current control method is cost effective, and does not have any adverse effect on the stability and the performance of the PV inverter. The new technique can easily be used in applications that use transformers, to reduce the core losses. The removal of the DC offset current has been achieved without sacrificing the overall conversion efficiency of the inverter system.

1.5 Publications Arising From Research

The following publications have been presented during the course of this research:-

[1] Sharma R, "Removal of DC Offset Current from Transformerless PV Inverters Connected to Utility", 40th International Universities Power Engineering Conference Proceedings, Sept. 2005 *(Proceedings available only on CD, ISBN 0-9502440-4-X).*

[2] Sharma R, Ahfock A, "Distortion in Single Phase Current Controlled PV Inverters for Grid Connection", Australasian Universities Power Engineering Conference Proceedings, Sept. 2004 *(Proceedings available only on CD, ISBN 1-864-99775-3).*

[3] Sharma R, "Switching Frequency Filter Design for Utility Connected PV Inverters", Australasian Universities Power Engineering Conference Proceedings, Sept. 2002 *(Proceedings available only on CD, ISBN 0-7326-2206-9).*

[4] Sharma R, "Analysis of PWM Transformerless Inverter for Utility Connected PV Applications", Australasian Universities Power Engineering Conference Proceedings, pp 195-200, Sept. 2001.

CHAPTER 2

REVIEW OF UTILITY CONNECTED PV SYSTEMS

2.1 Introduction

A review of research publications related to solar panels, batteries, the maximum power point tracker, the DC to DC converter and the inverter bridge with its voltage and current controllers is presented in this chapter. The purpose of this exercise was to identify potentially useful control methods, analytical techniques and their potential shortcomings when applied to the main components of single-phase utility connected PV system inverters.

Issues related to single-phase grid connected PV systems that were reviewed and presented in this chapter are divided into categories which: -

a) provided background information on operational issues including energy storage
b) reviewed operational aspects of single-phase grid connected photovoltaic systems
c) are devoted to maximum power tracking and DC to DC converters
d) covered switch-mode power factor controllers and reversible rectifiers which, although not directly related to PV systems, treat technical issues that are central to this project
e) dealt with power quality issues
f) covered issues related to DC offset current injection into the grid network
g) related to switching frequency filters

There were relatively few grid connected PV systems world wide prior to 1997 [2] and only a few Australian electricity authorities permit connection of transformerless

inverters to their supply systems. Therefore, the technical issues associated with transformerless inverter systems are still to be solved and publications related to the quality of power supplied by these systems were not available at the start of this project.

2.2. Solar Panels

PV panels are at present the most expensive part of the PV generation systems which constitute about 57% of the total cost [5]. However, PV panel manufacturers have become increasingly successful in producing higher capacity, higher efficiency PV panels at lower cost. Some believe that once PV systems enter the grid market, the cost of PV panels will significantly decrease [6, 7]. While there has been an increase in the number of grid connected PV systems, the reduction in cost of PV panels has not materialised. Despite the high cost of PV panels several Australian electricity authorities are evaluating utility connected PV generation. As stated in Chapter 1, increasing the efficiency and reducing the cost of the PV panels were outside the scope of this project and will not be discussed any further.

2.3. Energy Storages Batteries

Storage batteries used in PV systems are the second major contributor (approximately 30%) of the total cost of PV systems [5]. In PV generation which uses batteries for energy storage, proper management of battery charging, and selling any excess electricity to the authorities become important issues. The batteries are charged by both the PV generator and the utility during cheap off-peak periods and discharged during the peak consumer demand. Such a system described by Chiang, Chang and Yen [8] makes optimum use of the power available from both the PV panels and the conventional supply. The disadvantage of this arrangement is that the capital cost is high and the energy management system is complex. Other important economic issues such as battery maintenance cost and rate of return on capital [9-12] also need to be considered. Apart from economical benefits, there is a limit to the contribution to grid faults by utility connected PV systems without batteries. In PV generation,

fault current is limited to the short circuit current of the solar panels and is about 20% greater than its rated current. In this project, these benefits led to the decision to use the grid as effectively an infinite energy storage system rather then using storage batteries.

2.4. Utility Connected PV Systems without Batteries

In utility connected PV generation without batteries, the energy management system is much simpler because its function is to ensure that all the energy produced by the PV generator is instantaneously transferred to the grid supply. However, cloud movement influences the energy output from the PV panels and as such the voltage controller (responsible for managing the energy flow), has to respond to any intermittent loss in PV generation. The duration and magnitude of the intermittent loss in PV generation depends on the type of clouds and their speed of movement. It is assumed that variations with high rate of change are of low magnitudes. Jewell and Unruh have established that such variations, which may occur up to 15 times per minute, have magnitudes of the order of 5% of the installed PV generation capacity [13]. According to Jewell and Ramakumar [6], high magnitude variations (more than 50% loss of output) occur less frequently and have lower rates of change.

Power fluctuations due to cloud movement can lead to inverter stability problems in utility connected PV systems without batteries. A rapid rate of low magnitude power fluctuations requires suitable voltage controller design and is included as part of this project. The problems associated with the less frequent high magnitude variations or complete loss of power are deemed to be the responsibility of the supply authorities.

The less frequent fluctuations or complete loss of dispersed PV generation allows reasonable time for the control system of the conventional supply to respond. Limiting the total percentage of PV generation within the total generation mix can further reduce the possibility of any adverse effect due to the total loss of PV generation. For greater than 5% penetration, Sharma and Ahfock [14] have

established that some form of storage is required, if the frequency of the conventional supply is to remain within the required limits.

To cope with the high rates of PV power variation, the inverter voltage controller needs to be designed to maintain the voltage across the capacitor (v_c) constant (Figure 2.1(a)). The value of C should be large enough to keep the 100 Hz ripple content of voltage v_c within an acceptable level. The size of this capacitor will also influence the response of the voltage controller. There is therefore a need to investigate the relationship between the value of this bulk capacitance and: -

a) the response of the voltage loop to changes in the PV generator output
b) the response of the voltage loop to other disturbances such as starting of large motors
c) the response of the voltage loop to the inverter start-up and shutdown transients
d) the low frequency harmonic content in the inverter output current

2.5. Transformersless Utility Connected PV Systems

The success of this project depends on solving all the technical issues related to the connection of the inverter system to the mains supply without the use of 50 Hz power transformers (transformerless). Some electricity authorities in Australia (e.g. Pacific Gas and Electric Company) allow PV generators below 10 kW to be connected to their grid system without the use of power transformers. It has also been found by Chen and Divan [15] that the majority of low power (0.5-3.0 kW) line conditioning and uninterruptible power supply (UPS) applications did not require isolating transformers. While the information from these sources is applicable to this project, there was no published evidence to confirm that the DC offset current injected into the grid supply by transformerless PV inverters remains within the limits specified by the Australian Standards [4]. Hence, it was critical to the success of this project for the DC offset current controller to eliminate, or at least maintain the DC offset current

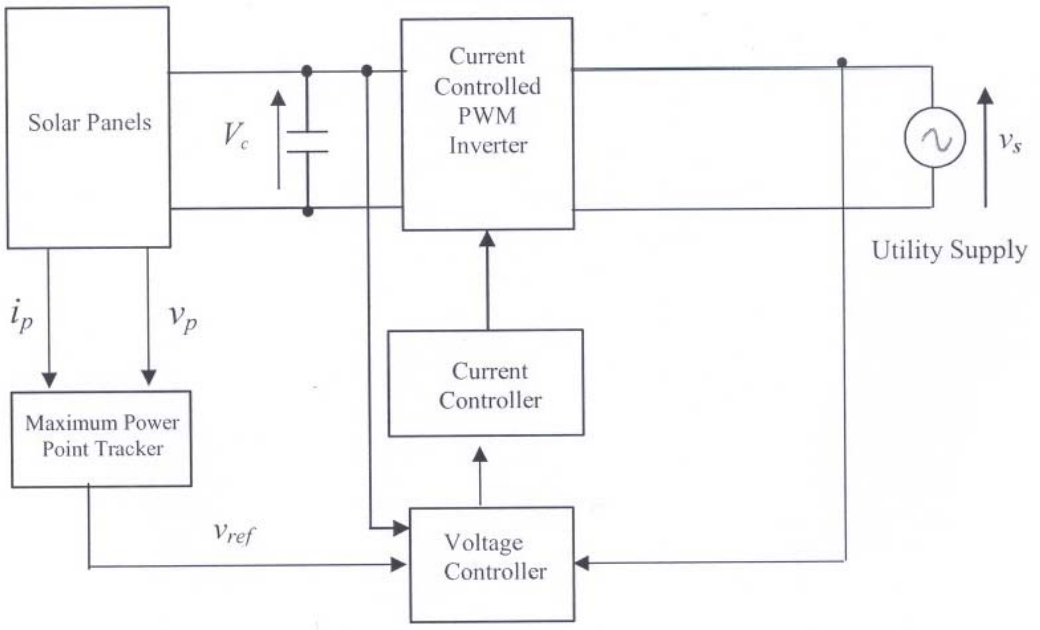
injected into the grid at acceptable levels, over the entire operating range of the inverter system.

2.6. Choice of Single-Phase Utility Connected PV Systems

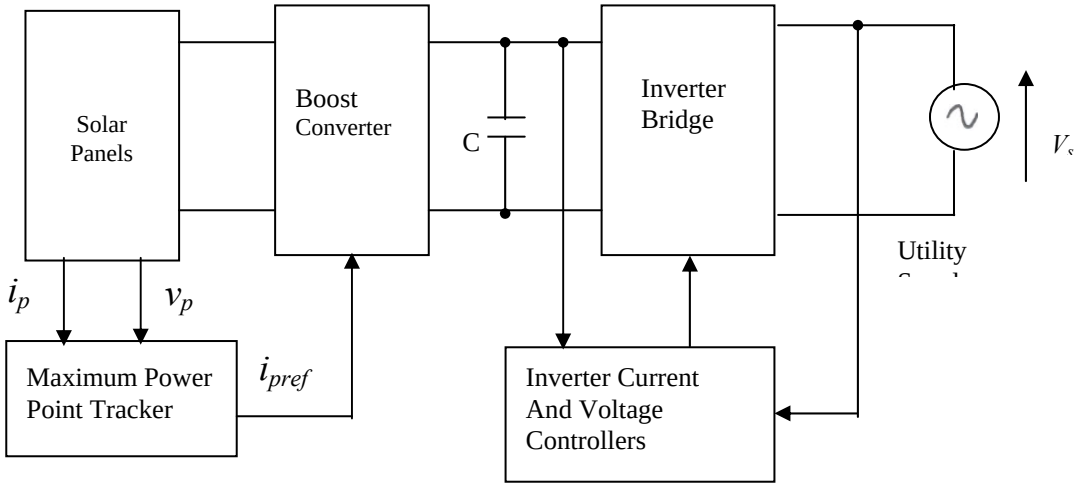
Different types of single-phase utility connected PV systems such as central inverter, string inverter, module integrated or module oriented inverters and the various inverter topologies have been analysed by Calais et al [16]. Of these different configurations, the module integrated inverter was considered to be the most suitable for the domestic PV application being considered in this project because it provided the most flexibility to design and test each stage separately. The main components of this type of single-phase utility connected PV system are shown in Figures 2.1 (a) and (b). These include the solar panels, the maximum power point tracker (MPPT), the DC to DC converter and the inverter bridge with its voltage and current controllers.

In order to achieve maximum efficiency, a photovoltaic energy conversion system normally includes a MPPT. As the temperature and/or insolation level varies, the location of the maximum power point on the generator's I-V curve changes. The function of the tracker is to ensure that the generator always operates at the maximum power point.

There are two possible ways to achieve maximum power tracking. In the single stage system shown in Figure 2.1 (a), the MPPT calculates and outputs a voltage reference (v_{ref}) that results in maximum power from the PV generator. The voltage controller adjusts the inverter output current so that the capacitor voltage (v_c) is maintained at the value dictated by the reference voltage. The main advantages of the single stage system are its low component count (no boost converter) and hence the likelihood of achieving higher efficiency.



(a): Single stage DC to AC conversion



(b): Two stage DC to AC conversion

Figure 2.1: Utility connected PV System Configurations

There is, however, a need for the minimum output voltage of the PV generator to be greater than the peak value of mains supply voltage. Also, the inverter must be

designed to handle the maximum output voltage of the PV generator that can be up to 50% greater than the minimum value. The possibility of the single stage system not meeting these requirements makes it unacceptable for the application being considered.

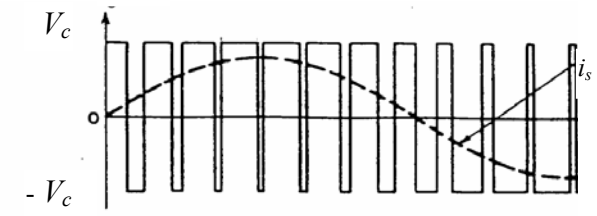
For these reasons and to give greater flexibility to design and test each stage separately the two-stage PV system in Figure 2.1(b) was adopted in this project. The tracker shown in Figure 2.1 (b) calculates and outputs a current reference, resulting in maximum power from the PV generator. The current controller operates the electronic switch in the DC to DC converter such that the PV generator output current is maintained at the optimum value as dictated by the reference current. The inverter extracts energy from the bulk storage capacitor (C) in such a way that its voltage is maintained at a constant value. The capacitor voltage has to be greater than the peak value of the supply voltage to minimise current distortion.

In the proposed inverter system, as stated earlier, the voltage controller is responsible for keeping v_c constant. It achieves this by ensuring that all the power produced by the PV panels is transferred to the grid system. The voltage controller controls the power flow by controlling the magnitude of the output current (i_s).

The function of the current controller is to produce a sinusoidal output whose magnitude and frequency can be controlled. It does this by forcing the current from the PV panels to stay within a tolerance band around a sinusoidal reference current, provided by the voltage controller.

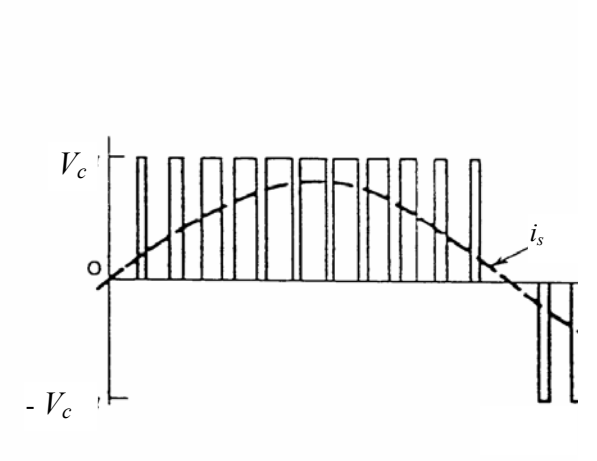
As stated in Chapter 1, to reduce the losses, cost and size of the inverter system, it was decided not to use current loop configurations in which a power transformer is essential. Other types of inverters such as single-phase half bridge inverters with two capacitors connected across the input DC source were considered not suitable. Without the use of a step-up transformer, this type of half-bridge would need to be supplied with twice the DC voltage from the boost converter compared to the full bridge configuration. This method was therefore considered unsuitable and hence, the single-phase full bridge inverter was chosen.

With the single-phase bridge, using the pulse width modulation (PWM) scheme, the electronic switches in the current loop can be switched using either the bipolar or the unipolar mode. In the bipolar mode, the diagonally opposite switches of the two legs of the inverter bridge are switched as pairs. The output voltage swing (v_c) is shown in Figure 2.2 (a). In the unipolar mode, the two legs of the bridge are not switched simultaneously but are controlled separately. Figure 2.2 (b) shows the inverter output voltage. In the unipolar mode, the output voltage swing is half of that in the bipolar mode for the same input DC voltage.



(a): bipolar voltage switching

(Adapted from Power Electronics, 2nd Edition, John Wiley & Sons, page 212 by Mohan, Undeland and Robbins)



(b): unipolar voltage switching

(Adapted from Power Electronics, 2nd Edition, John Wiley & Sons, page 216 by Mohan, Undeland and Robbins)

Figure 2.2: PWM with unipolar and bipolar voltage switching

2.7. Operating Principles of Single Phase Inverter Systems

The current controlled method was chosen over the voltage controlled method. Current control offered advantages such as active current wave shaping, direct control of real power flow, control of harmonic currents injected into the mains, inherent

current limitation and automatic synchronisation with the utility grid (Borle, Dymond, Nayar and Phillips [17]).

Figure 2.3 shows a simplified diagram of the inverter current control loop. Hysteretic control is used to force current i_s to track the reference current i_{sref}. The controller forces the bridge into one of four of the possible states depending on the need to make $|i_s|$ rise or fall and on the polarity combination of the v_s and i_{sref} signals. Figure 2.4 and its accompanying table illustrate this point. Since power flows from the DC side to the AC side, the bridge behaves like a buck (step-down) converter. Current $|i_s|$ is made to rise by switching on T_{A+} and T_B- if v_s is positive or T_{B+} and T_A- if v_s is negative. During this time i_y is equal to $|i_s|$ and capacitor C discharges. To make $|i_s|$ fall one of the previously conducting electronic switches is turned off. During this time i_y is equal to zero. Since the reference current i_{sref} provided by the voltage control loop is in phase with the mains voltage v_s, the bridge operates in the inverting mode at unity power factor. A more detailed explanation related to switching options available is provided in chapter 4.

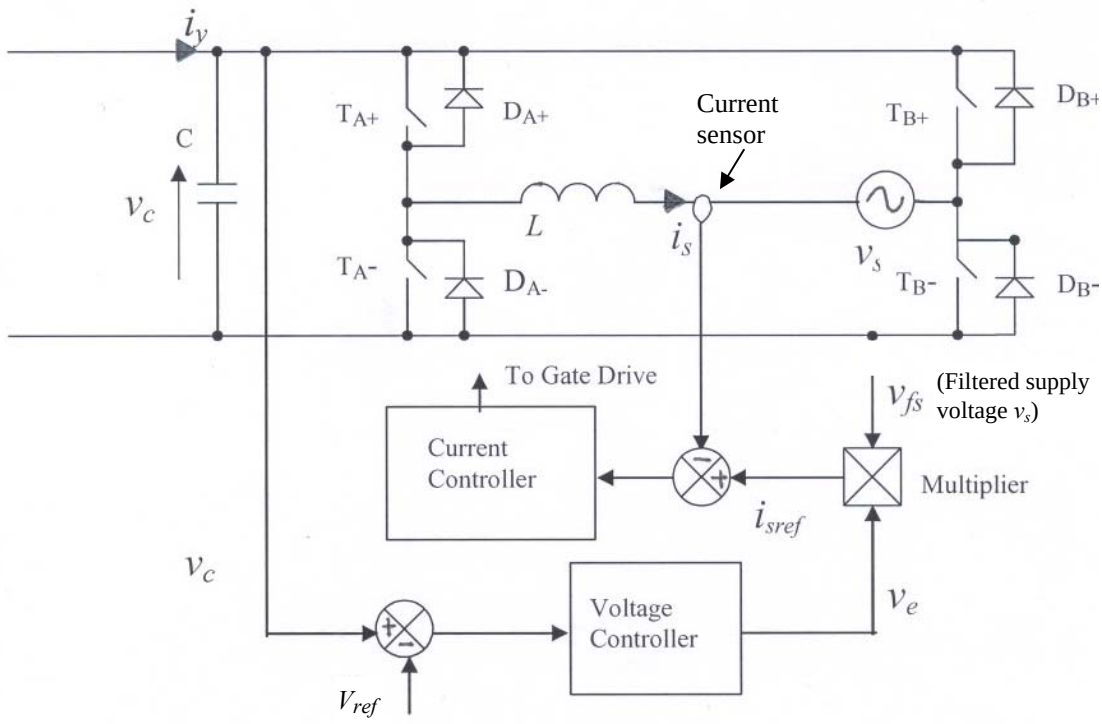
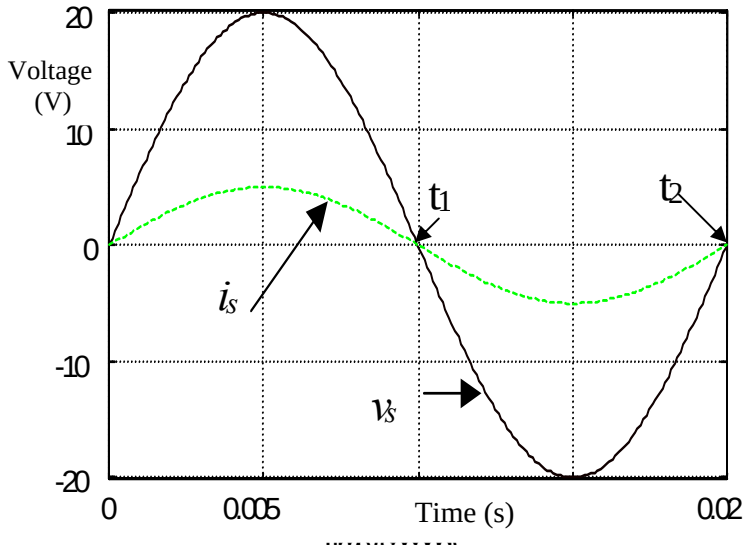


Figure 2.3: Simplified diagram of inverter current and voltage control loops

As mentioned earlier the aim of the voltage control loop is to keep the capacitor voltage V_c constant. The value of C must be carefully chosen as it affects the dynamic response of the voltage controller and also the amount of low frequency harmonic currents in i_s. Failure to do so may lead to excessive overshoot in DC voltage V_c and generation of unacceptable levels of third harmonic currents.

It has also been mentioned by Calais et al [16] that not only the cost and the efficiency but also the lifetime of the inverter system is influenced by the size of the electrolytic capacitor C. It is for these reasons that a design procedure for the voltage control loop that yielded an optimum value of C was necessary.



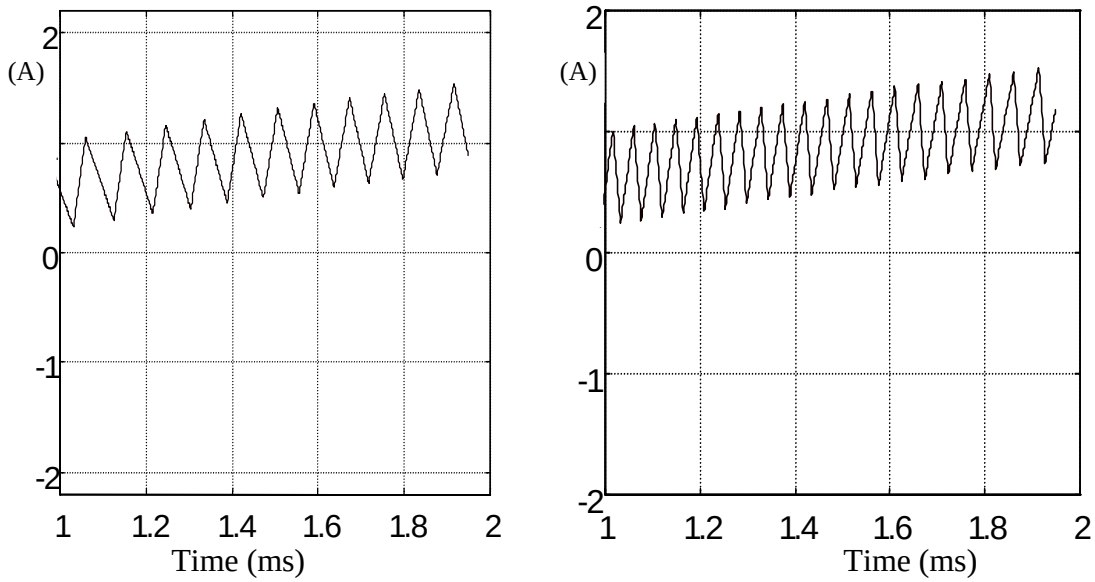
Time interval	$0 \rightarrow t_1$	$t_1 \rightarrow t_2$
Polarity of v_s signal	+	–
Polarity of i_s signal	+	–
Devices conducting	T_A+, T_B-	T_B +, T_A-
Devices conducting	T_A+, D_B+ or T_B -, D_A-	T_B +, D_A+ or T_A -, D_B -
Direction of power flow	DC ⇒ AC	DC ⇒AC

Figure 2.4: The four states in inverting mode.

2.7.1. Unipolar and Bipolar Switching

To obtain a near sinusoidal current from the inverter, it is common practice to use a dedicated current control loop. The function of the current loop is to select the appropriate inverter transistors and switch them on for a precise duration. A carrier based switching method or a direct current control technique, such as the hysteretic method can be used. Hysteretic control was chosen because of its simplicity.

Since the voltage swing across the inverter output is halved in the unipolar mode (Figure 2.2), theoretically, the switching frequency is also halved provided the tolerance band, filter inductance and the inverter input DC voltage remain constant, as shown in Figure 2.5. Consequently, for a given range of switching frequencies, the value of the inductance required in the unipolar mode is half that of the value of inductance needed in bipolar mode.



(a) Unipolar switching (b) Bipolar switching

Figure 2.5: Inductor current from a single phase inverter

From the preceding explanations, two points can be made, both of which have direct bearing on the amount of power loss. Firstly, with bipolar operation there are two transfers of currents between electronic switch pairs per switching event, whereas with unipolar operation there is only one. This 50% decrease in current transfers per

switching event translates into lower switching losses in the unipolar case. Secondly, since a smaller filter inductance is needed, for a given switching frequency in the unipolar case, power loss associated with the inductor is reduced for a given amount of copper and core.

There is however, some concern about the current distortion on either side of the zero crossing. With reference to Figure 2.3 the rate of rise of inverter output current i_s is given by equation 2.1. In the unipolar mode, when the current is decreasing, equation 2.1 can be simplified to give equation 2.2. As the voltage V_s approaches zero, $sin\ \theta$ approaches zero. Equation 2.2 suggests that inadequate switching may occur near the current zero crossing, and this may give rise to unacceptable levels of low frequency current harmonics and ripple current filtering problems.

$$\frac{di_s}{dt} = \frac{V_c - \hat{V}_s \sin\theta}{L} \tag{2.1}$$

$$\frac{di_s}{dt} = \frac{-\hat{V}_s \sin\theta}{L} \tag{2.2}$$

where $\theta = \omega t$

Therefore, detailed analyses of both the unipolar and bipolar modes are required. The suitability of using a unipolar controlled bridge would be based on the outcome of this analysis.

Maximum or peak efficiencies of commercially available inverters typically are greater than 90%. In most applications, it could be argued that such high levels of efficiencies are satisfactory and further improvements, although possible, are not cost effective. However, in PV applications, the incentive to improve efficiency is stronger not only because of the high cost of PV power but also because PV systems operate at peak power for only short periods during the day. It is therefore, important not to waste that power during the DC to AC conversion process. For an example, a design improvement costs *x* dollars and reduces power losses by 1W, then that improvement is cost effective if *x* is less than six dollars. Hence, any improvements in inverter efficiency must not be accompanied by an increase in cost or a compromise in the quality of power from it.

This situation provided the motivation to revisit inverter systems, control techniques and filtering methods with the aim of identifying any configurations or control strategies with potential advantages from energy and cost saving points of view.

2.7.2. Maximum Power Point Tracking

Wolf and Enslin [18] have suggested that in some applications, it is possible to obtain as much as 30% cost reduction by using a high efficiency (96%) maximum power point tracker (MPPT) with PV systems [18]. While MPPT and the DC to DC boost converter is part of the overall PV system, they were not the main focus of the research in this project. However, it is necessary to explain the operation of MPPT and DC to DC converter because its matching function allows maximum power to be transferred from the PV panels to the gird system. The MPPT and DC to DC converter configuration chosen are shown in Figure 2.6.

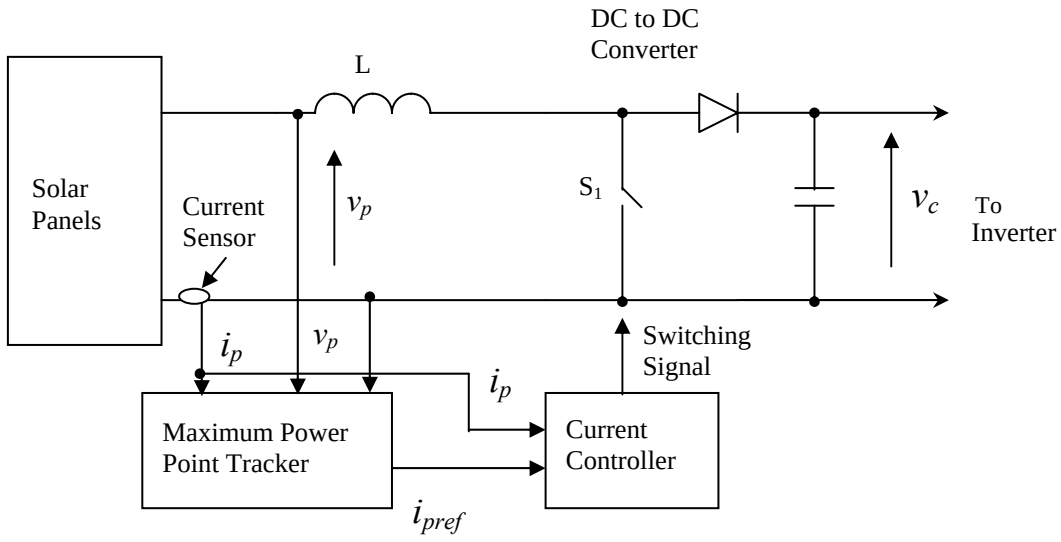


Figure 2.6: DC to DC Converter with MPPT

The typical I-V characteristics of a solar panel as the insolation and/or temperature changes are shown in Figure 2.7. The maximum power points (MPP) for these three curves, occur at A, B and C. The function of the maximum power point tracker is to ensure that the PV system is always operating at the MPP on the I-V characteristics

irrespective of the temperature or insolation level. Depending on the temperature or insolation level, the reference current (i_{pref}) is continually adjusted so that maximum power is obtained from the panels. The current controller provides the switching signal to electronic switch S_1 so that the output current (i_p) supplied to the inverter, is forced to stay within a small tolerance band around i_{pref}. When S_1 is on, diode (D) is reverse biased and i_p increases. When S_1 is off, i_p decreases as energy is transferred from the PV panels and the inductor L to the inverter. In practice, MPP is achieved by controlling only one parameter of the DC to DC converter, that is, the duty cycle of the switch S_1.

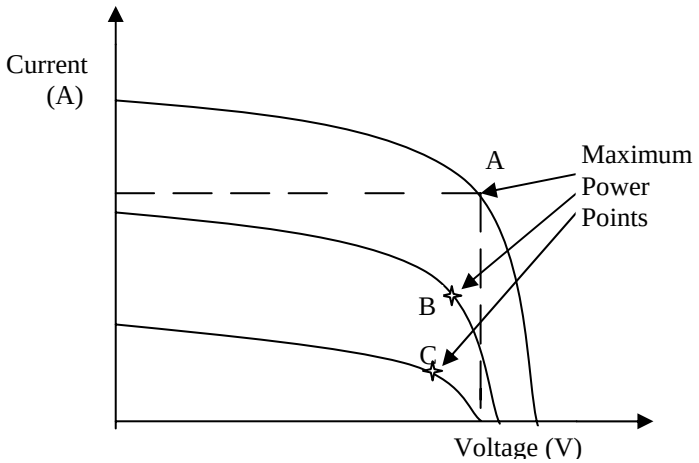


Figure 2.7: I-V Characteristics of a solar panel

The MPPT continuously calculates the PV output power and compares this with the power measured at a previous instant to decide whether i_p should be either increased or decreased. This process continues until the maximum power point is reached. At the optimum power point, the current oscillates above and below the optimum value. Salameh and Taylor [19], used an analogue multiplier to calculate the instantaneous power and the power comparison process to determine the optimum value was carried out using two simple RC circuits. The response of this method is slow and is therefore less efficient than the microprocessor-based system used by others [20-22]. The advantages of using a microprocessor are that not only has it become relatively cheap

but that it also performs both the multiplying and comparing functions much faster. Therefore the maximum power point is reached at a faster rate.

A microprocessor based MPPT and DC to DC converter with efficiencies greater than 98% was designed, constructed and tested by Sharma and Bowtell [22], and is presented in Appendix A. As stated earlier, this stage of the overall utility connected PV system will not be considered any further because the main focus of this project is minimising power loss of the inverter.

2.7.3. Current Control Loop

It is relatively easy to find research publications on single-phase, bi-directional bridge rectifiers, using bipolar switching [23-28]. However, based on the extensive review of published literature, papers that specifically deal with hysteretic current control, transformerless, unipolar switched inverters that are for utility connected PV systems were difficult to locate.

It has been published by Jiang and Brown [29] that rapid changes in voltages and currents due to switching action within converters are a source of Electromagnetic Interference (EMI). However, one advantage of unipolar switching mentioned earlier is lower DC voltage jumps and subsequent reduction in power loss [30]. This reduction in voltage transitions during switching is therefore an advantage from the point of view of EMI generation. In this project however, to minimise the effect of EMI on other equipment connected to a point of common coupling (PCC), other methods to improve the quality of the power delivered by PV inverters required further investigation.

Apart from choosing the most appropriate switching mode, a decision also had to be made on the type of current control technique suitable for this project. The PWM, hysteretic current control strategy with fixed-band tolerance was chosen over ramp-comparator current control. In the ramp-controller technique, the current error is compared with a triangular carrier waveform to provide the switching signal for the inverter power switches. The advantage of the ramp-controller technique is that the

switching frequency is governed by the carrier frequency and the harmonics are at a fixed frequency. The disadvantage of this method is that the system response is affected by the stability of the feedback loop and as a result, phase and amplitude error exists even at steady state (Rahman et al [31]).

One of the advantages of the PWM hysteretic control technique is that lower order current harmonics are eliminated [16]. However, this is only true in an ideal situation where no circuit delays exist. A practical current control loop (CCL) cannot be constructed with zero circuit delays. It has been shown by Dodson, Evans, Tabatabei and Harley [32], that even intentional delay such as *'dead time'* introduces low order harmonics. There is no published evidence to show that the lower order current harmonics generated (due to implementation delays) by unipolar switched inverters using this current control strategy could be maintained within the legal limits specified by Australian Standard 4777.2, 2005 [4].

It has also been shown by Tungpimolrut et al [33] that with the presence of large delay, the average switching frequency of a hysteresis current control bipolar switched inverter will decrease causing the total harmonic distortion (THD) to increase. While the results presented by Tungpimolrut et al [33] were for a three phase bipolar switched inverter supplying a three phase induction motor, they are relevant to this project. However, knowledge of the level of low frequency harmonics, essential for utility connected inverter systems, was not provided.

Therefore, to achieve the aims of this research, the relationship between unavoidable switching circuit delays or implementation delays (blanking time, dead time, unwanted propagation delays) and the level of low frequency current harmonics generated by the proposed PV inverter system will be analysed in Chapter 3. The total implementation delays of a PV inverter system can be in the range of a few microseconds to tens of microseconds. Actual measurement of implementation delays will be carried out in Chapter 4.

The disadvantage of hysteretic current control is that the switching frequency varies along the current waveform and according to Ghosh and Ledwich [34] the choice of

hysteresis band is a compromise between tracking error and inverter losses. For the purpose of designing filters, it is important to be able to predetermine the switching frequencies. Knowledge of the switching frequencies allows designers to prevent the resonance frequency of the AC filter network from coinciding with the switching frequencies. The choice of switching frequency is also a trade off between switching loss and the distortion of the output current. It has also been suggested by Boys and Green [24] that if the average switching frequency is kept above 2 kHz, then the resulting distortion should be of little concern to the power supply authorities. Therefore an analytical method that includes implementation delays will be developed in this project to determine the current loop parameters such that all these requirements are met.

Another disadvantage of hysteretic current control identified by Brod and Novonty [35] was the problem of interference in three phase inverters. The switching pattern of each phase was influenced by the other phases and limit cycles always existed. Various methods have been used to overcome these problems:-

i. space vector [36-38]
ii. constant frequency modulation [39 and 40]
iii. variable hysteresis band methods [41-43]
iv. superimposing a common offset signal [33].

While these interference problems are related to three phase inverters, solutions such as the use of variable the hysteresis band method to minimise unwanted switching is applicable to this project. Simple solutions to minimise interference due to the switching action need to be investigated for the single phase transformerless inverter system proposed in this project. Failure to prevent interference may result in unwanted switching, and in the worst case, short circuit of the inverter input DC supply.

Finally, the stability of the current loop, with a switching frequency filter and a DC offset current controller, also required further investigation. It was decided that a comparison of the amplitudes of the low frequency harmonic currents using the two

modes of switching, would determine the most appropriate switching mode for this project.

2.7.4. AC Filter

Although the frequency of the harmonic currents injected into the AC mains ranges from low to very high frequencies, there are three groups of frequencies with amplitudes large enough to be of concern to supply authorities. These groups include low frequency harmonics (multiples of 50 Hz), switching frequency harmonics and high frequency harmonics.

The low frequency harmonics are reduced below levels specified by Australian Standard [4] by the use of sinusoidal PWM and appropriate design of the voltage control loop. The presence of stray capacitance and stray inductance in the current control circuits give rise to high frequency current harmonics (usually in the hundreds of kHz to MHz range). In order to meet the EMC standards, these harmonics can be reduced by using a radio frequency interference (RFI) filter and, during implementation, by using good circuit layout and design. Harmonic filters for RFI reduction are commercially available.

Harmonics also exist around the switching frequencies of the inverter. These are in the kHz range. The level of current distortion caused by these harmonic currents may be of concern to the supply authorities. Growing numbers of distributed renewable energy generation use inverters with electronic switches to switch currents at high frequencies. This gives rise to potential waveform distortion and the risk of harmonic resonance that could lead to the destruction of shunt capacitors. To minimise such problems, there are several national and international standards that govern the acceptable level of current distortion. The IEEE standard [44] limits the maximum total harmonic current distortion (THCD) to less than 5%. There are other Australian Standards [45] that govern the level of current distortion at the output of AC filters. As these standards become increasingly stringent, and the technology to switch large currents at high frequencies continue to improve, the need to filter the switching frequency current harmonics has to be taken seriously.

Switching frequency current harmonics can be reduced by using a tighter tolerance band together with higher current control loop (CCL) inductance or by using a separate filter. Some of these methods would lead to large additional power loss, which is not desirable. An important requirement of a switching frequency filter designed for this project is that it should achieve attenuation of the ripple current without compromising the efficiency of the inverter system. Therefore existing filter designs needed to be evaluated to identify suitable AC filter arrangements for this project.

Passive and active power filters have been widely used to reduce current harmonics and also to compensate reactive power. The advantage of active power filters is that they offer better output regulation with very fast response and are smaller in size. The cut-off frequency of the active filter governs the order of harmonics that can be suppressed. It has been shown by Dastfan, Gosbell and Platt [46] that active filters have no limit to the order of harmonics that can be attenuated. The disadvantages of this method are:

- a large number of active components are required
- complex algorithms may be required to control several switches
- in certain situations they may act as negative resistances and hence amplify the existing harmonic content in the supply system
- increased cost

In the domestic PV inverter system being considered, apart from power losses, the filter needs to be simple in design and low in cost. It was decided that active filtering was not a suitable option because of complexity and cost. Instead, passive filtering would be considered for this project.

Passive filters are simple to design and usually consist of a series inductor and a shunt capacitor connected to the inverter output. The inductor is rated to carry the rated load current and may lead to significant additional power loss, which is not desirable. To maintain stability these arrangements often require some form of damping. Different filter configurations using resistor damping, and their merits and demerits have been

well documented by Valtkovic, Borojevic and Lee [47]. All these different types of filter configurations have at least one of the following disadvantages: -

- excessive damping resistor power dissipation
- poor high frequency attenuation capabilities
- excessively large filter components

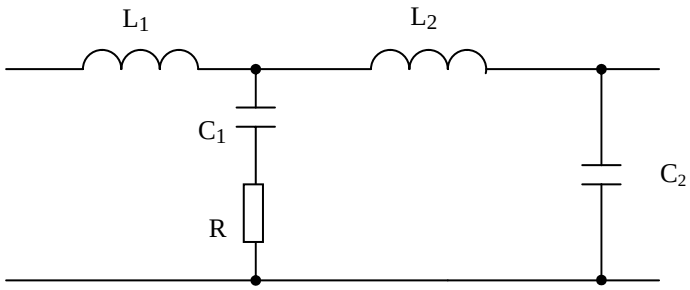


Figure 2.8: Passive filter with pole damping

Figure 2.8 shows one of these filter designs [47] that was considered suitable for DC to DC converter applications but not in AC power converter applications. The reason being that for effective damping C_1 has to be large (at least ten times C_2) and therefore with 50 Hz mains voltage across the series R and C_1 combination, the power dissipated by damping resistor R can be relatively high. However, for the ripple current filtering being considered in this project the value of C_1 need not be large if the minimum switching frequency is greater than 2 kHz. Therefore, the suitability of such a filter and its effect on the performance of inverter systems will be further investigated in Chapter 5.

Senini and Wolfs [48] have also presented an alternative method of switching frequency filtering. They have used a simple technique called '*ripple steering'*. A coupled or modified inductor with a main winding L_1 and a second auxiliary winding L_2 for ripple steering is shown in Figure 2.9. In simple terms, the second inductor winding in series with capacitor C_1 provides a low impedance path at the ripple frequency. The steering action is achieved by choosing the inductor turns ratio such that most of the ripple current is diverted to the additional winding. This simple approach requires only a small increase in copper and an additional capacitor to carry

the ripple current. The disadvantage of this method is that any small error in the turns ratio may result in ripple current being injected into the supply. Increasing the leakage inductance will decrease the sensitivity to the turns ratio error and hence this problem may be reduced. Also in the boost converter application by Senini and Wolfs [48] the switching frequency is reasonably constant, while in the hysteretic current control inverter systems to be considered in this project, the switching frequency varies along the current waveform.

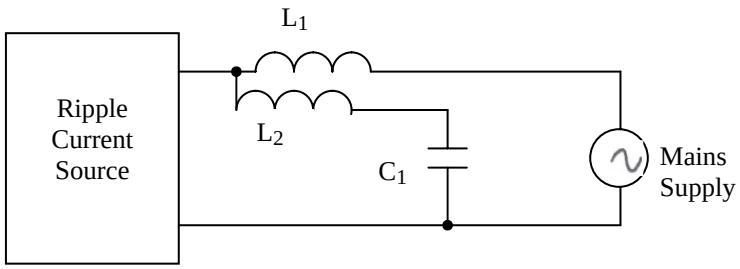


Figure 2.9: Ripple current steering.

Therefore, while the simplicity of the ripple current steering method is an advantage, there is a need to investigate the use of this technique on the AC side of the inverter to determine the effects of: -

- the AC voltage across the current steering winding on the performance of the filter
- large variations in the switching frequency on effectiveness of the ripple steering technique
- the impedance of the mains supply on the performance of the filter

The ripple current steering technique (without auxiliary winding) and a modified passive filtering circuit such as the arrangement shown Figure 2.8 will be further analysed for use in this project.

Based on the literature review, aspects of the current loop that needed further investigation include: -

- determining if unwanted interaction problems existed between the current controller, the voltage controller of the inverter system and the switching frequency filter
- identifying the sources of the DC offset current component present in the inverter output current, and if required, developing methods to remove it.
- determining the effects of implementation delays on switching frequencies and hence on the performance of the current controller and the switching frequency filter.
- determining the effects of the switching frequency rejection filter on the response of the current controller
- determining the effects of the PV array earth capacitance on the performance of the inverter in transformerless PV grid connected systems

According to Calais et al [49], PV array earth capacitance can cause interference. The resulting earth leakage current, may lead to unwanted tripping of the earth leakage circuit breakers. However, addressing this problem will not have any bearing on the conversion efficiency of the inverter. For this reason the effects of the PV array earth capacitance on the performance of the inverter system will not be dealt with in this project.

2.7.5. Voltage Control Loop

Voltage control loops similar to the one shown in Figure 2.10 have been analysed by several authors [23, 28]. The problem of low frequency harmonics in rectifier applications, resulting from multiplication of the harmonics present in v_c by the sinusoidal signal, was recognised by Omar and Boon-Teck [23]. The problem was solved by the inclusion of a low pass filter (A) as shown in Figure 2.10.

The voltage loop can employ either a proportional integral (PI) controller or a proportional (P) controller to keep the input voltage v_c constant. PI controllers have been used in situations where an effective steady state voltage regulation was essential [23, 24]. While proportional control has a steady state error, it does display

better dynamic response than PI control. It has been found [24] that the simple proportional feedback control had excellent characteristics such as: -

- the DC voltage is always maintained above the peak AC voltage thereby minimising the possibility of the current being distorted
- the rectifier power is matched almost instantaneously to the load demand

These features are relevant to this project because all the energy produced by the solar panels has to be instantaneously supplied to the grid system. Also, it would be more acceptable to the supply authorities if the DC voltage was less likely to fall below the peak AC voltage, and cause current distortion.

Despite its disadvantage (steady-state error), the proportional feedback control was worth considering for the utility connected PV generation system. The error can be tolerated because the increase in DC voltage coincides with an increase in the inverter output current i_S which would help keep the distortion in i_S at an acceptable level. Simulations of the voltage loop will be carried out in this project to confirm the benefits of using P-controller instead of the more commonly used PI-controller.

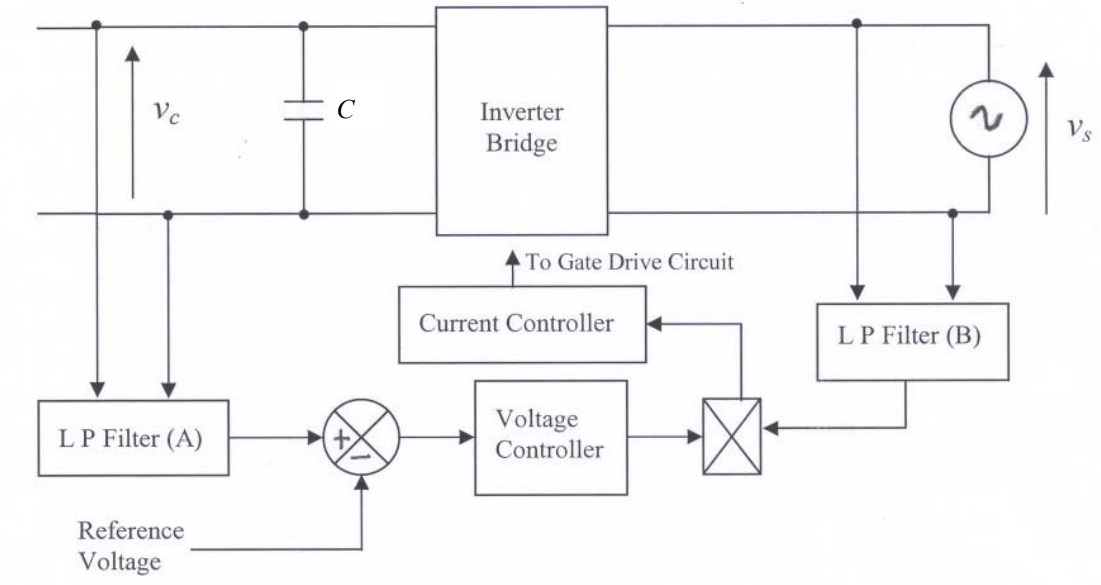


Figure 2.10: Voltage control loop

The design of the voltage loop is critical and as discussed in chapter 1, failure to do this properly may result in v_c rising to dangerous levels. Linearised models have been developed [22, 23 and 28] for the voltage loop based on assumptions such as: -

- the inverter was considered to be ideal
- the current loop was assumed to be perfect
- the hysteretic band was assumed to be small and therefore, the ripple current effects were ignored.

These assumptions are applicable to this project. However, only Hava, Lipo and Erdman [28] included a design procedure. Unfortunately, this design procedure did not include the low pass filter (A) to reduce the 100 Hz ripple present in v_c and this is an essential feature that had to be included. The product of the 100 Hz ripple and the attenuated 50 Hz voltage v_s produces third harmonic currents. In utility connected PV generation these third harmonics need to be maintained below 4% of the fundamental value [4]. Therefore, the low pass filter (A) cannot be ignored when developing the design procedure. Also in this design procedure [28] a PI feedback control is used whilst a proportional feedback control is to be evaluated for use in this project. Consequently, the analysis of the voltage loop for the utility connected PV system should include: -

- a systematic design procedure based on a linearised model which returns values of the capacitor C, the time constant of the low pass filter for a specified value of 3rd harmonic content in i_s

- estimation of the 3rd harmonic currents (introduced by the voltage loop) for given values of steady state error in the DC input voltage v_c

- a dynamic response of the voltage controller to represent the effects of cloud movement

- a response of the voltage controller to changes in the utility supply voltage to represent a large load being switched on.

2.8. Power Quality

Power quality problem has been defined by Dugan et al [50] as: *Any power problems manifested in voltage, current or frequency deviations that result in failure or misoperation of customer equipment*. The PV inverter designed in this project is a non-linear device that generates current harmonics, which can lead to the distortion of the supply voltage and current. The serious consequences of the distorted supply voltage and current on the neutral conductor, and on performance of sensitive equipment have been discussed by other researchers [51 - 56].

The level of current harmonics generated by common non-linear devices such as energy efficient fluorescent lamps, televisions and computers, has been documented by Herman et al [54]. They range from 25% to 90% for the 3^{rd} harmonic, to 20% to 50% for the 9^{th} harmonic. A single non-linear device with such high levels of 3^{rd} harmonics may have no impact on the supply voltage. However, when large numbers of non-linear device such as computers are connected to the supply system it may cause distortion of the supply voltage. Figure 2.11 illustrates the effect of non-linear loads on the supply voltage.

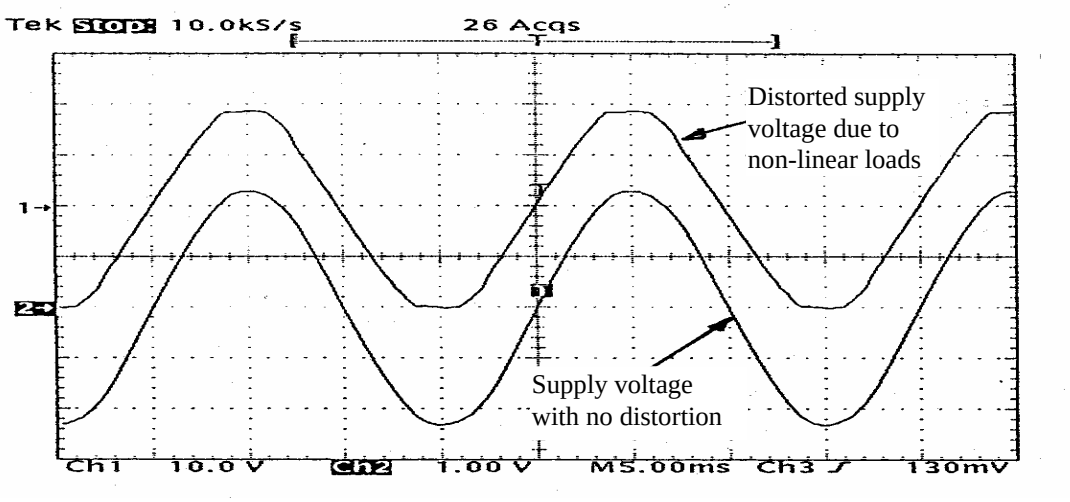


Figure 2.11: Supply voltage distortion due to non-linear loads.

The Australian Standard [4] limits 3rd harmonics injected into the grid by PV inverters to 4% of the fundamental value. For a 1 kW inverter system operating at unity power factor, this would translate to about 0.167 A. As an example consider the 665 1 kW inverters in the Solar Olympic Village in Sydney, operating at below (eg 3%) the legal limit and generating 0.125A of 3rd harmonic current. This would mean a total current of about 83 A in the neutral conductor. The power loss associated with this large current would lead to the extra heating of the neutral conductor and the three phase transformer supplying the village. This example illustrates that power quality influences power losses and hence the cost of the power distribution system.

It is for the above reasons that the quality of power supplied by the inverter designed in this project is being considered as a critical issue.

2.9. DC Offset Current Elimination

If inverters are to be directly connected to the grid (without power transformers) then the level of DC offset current injected into the grid should not exceed the legal limits of 5 mA or 0.5% of the rated current (whichever is greater) [4]. Keeping below this limit will minimise accelerated electrolytic corrosion of the earthing conductors, and

prevent power distribution transformers that normally operate near saturation from going into saturation [57].

The sources that are likely to contribute to the presence of DC offset current at the output of inverters include:-

- the impedance of the two arms of the inverter-bridge not being perfectly equal;
- DC offset present in the reference current; and
- DC offset introduced by feedback current sensors.

To be able to control the DC offset current injected into the grid supply, the first major problem is to measure small components of DC current (usually in the tens of milliamperes) from a large AC current (above 4 A in this project). It has been shown by Masound and Ledwich [57] that the small resistance of the inverter outer loop was sufficient to use with a simple RC circuit to provide the necessary level of voltage feedback to the current controller. The advantage of this method of measuring the DC voltage (due to DC offset current) is that it does not introduce additional DC offset current. The disadvantage of the method used by Masound and Ledwich is that it failed to provide adequate separation of the DC voltage from the AC voltage. It was also shown that adding an integrating stage to the RC output did not provide adequate reduction of the AC ripple component [57]. This was not acceptable in the proposed project because the presence of an AC ripple current in the feedback signal may not only make it difficult to remove the DC offset current, but may also introduce additional switching problems.

Despite an exhaustive literature review, there was no evidence that the DC offset current from PV inverters injected into the grid can be economically and efficiently maintained at an acceptable level. Therefore new techniques to separate the DC offset current from the AC current and then maintain it within the legal limits may need to be developed.

2.10. Conclusions

Based on the literature review carried out in this chapter, it was found that: -

- market surveys indicate that some electricity consumers are willing to pay extra for renewable energy;

- the design of the inverter voltage control loop must take into consideration the effect of the PV generation power fluctuations and other disturbances;

- the ripple current steering technique is potentially an efficient method of filtering switching frequency harmonics, but its suitability for unipolar switched inverter applications and the use of other simple circuit configurations required further investigation;

- there was a need to investigate the effect of circuit delays on the performance of the current controller in both the bipolar and unipolar switching modes;

- the advantage in improved efficiency of inverters using unipolar switching has been recognised. However, other potential benefits of using this switching strategy need to be explored;

- the potential for using a switching frequency rejection filter, and the effect of implementation delay on the filter performance as switching frequency varies along the current waveform, both require investigation;

- new methods to separate and remove the DC offset current from the AC current present in the output of a transformerless inverter may need to be developed;

- the voltage and current control techniques used in power factor controllers and switch-mode rectifiers are applicable to the inverter being designed for utility connected PV systems. However, the interactions between these loops need to be investigated to establish if they can be designed separately.

In conclusion, the review of current relevant literature has revealed an absence of published material for transformerless, hysteretic current control, unipolar switched inverters for utility connected PV application that included switching frequency filtering. None of the published inverter design processes incorporated implementation delay and its effects on performance, power quality, efficiency and cost of inverter systems. Finally, there is no published data giving typical values of DC offset current generated by transformerless inverter systems or establishing the need for a DC current controller.

Since the largest source of power loss is the current control loop, its design will be critical to the success of this project, and hence this will be carried out in the next chapter.

The power loss of the voltage control loop is insignificant when compared to that of the current control loop. However, its performance does influence the quality of the power injected into the grid system and hence its design is carried out in Chapter 6.

Finally, islanding is a phenomenon that relates to the independent operation of grid connected PV inverters during the absence of the conventional power supply. A number of self-activated inverters form an "*island*" when the grid supply has tripped due to a fault condition or been turned off for maintenance. In such situations a major problem to be avoided is unwanted variations of inverter output frequency and voltages, and danger to uninformed maintenance personnel. The inverter control systems to be designed in this project is to establish if unipolar switched transformersless PV inverters can be realised. If for any reason the mains supply tripped, the inverter output would be isolated from the grid supply and the input DC voltage would automatically be disconnected. The inverter system is switched off because the loss of the grid supply means that no additional energy is available to bridge the energy gap between the varying PV energy output and the consumer energy demand. Therefore, it is not practically possible to meet the power needs of a consumer without the grid supply and without storage batteries. Hence, with the inverter system isolated in the event of mains supply failure, islanding becomes a non issue.

CHAPTER 3

CURRENT LOOP: UNIPOLAR VERSUS BIPOLAR SWITCHING

3.1. Introduction

The need for technical improvements in the design of inverters for grid connection, to achieve higher conversion efficiencies without compromising the output quality, was established in chapter 1. To implement these technical improvements, existing current control techniques, switching strategies, voltage control techniques, AC filter designs, DC offset current elimination techniques, and other issues related to utility connected PV generation were reviewed in Chapter 2. To improve the efficiency of inverter systems, several key issues associated with the current control loop (CCL) were identified for further research during this review process.

In this chapter, theoretical modelling and simulation results of the CCL without the DC offset control loop and switching frequency filter (SFF) are presented. In inverter applications where transformers are used, control of DC offset current is not an issue, and there are also situations where use of AC filters to attenuate switching frequency current harmonics is not necessary. As such, the CCL with the SSF included, and the DC offset current controller, will be considered separately in Chapters 5 and 8 respectively. This will allow the current loop design procedure developed in this chapter to be used in other applications.

The exhaustive literature review carried out in Chapter 2 provided no evidence that use of unipolar switched inverters would result in acceptable levels of current harmonics injected into the grid system. It was therefore necessary to confirm whether unipolar switching is inferior to bipolar switching in terms of low frequency

harmonic currents injected into the mains supply. The likelihood of inadequate switching near the current zero crossing, and its effects on the quality of power delivered by unipolar switched inverters, was also of concern. Hence a detailed evaluation of the current loop using both the unipolar and the bipolar switching modes is carried out in this chapter. A design procedure for the current loop using the preferred switching mode based on the results of this evaluation is also presented.

The aim of the design process of the CCL carried out in this chapter is to yield control loop parameters that should optimise inverter efficiencies, without compromising the quality of power delivered by the inverter system. Developing a relationship between efficiency, power quality and implementation delay makes this design process novel.

The theory and the simulation results to be presented include: -

a) a detailed evaluation of the current loop using both bipolar and unipolar switching modes.

b) a new design procedure for the current loop that returned component values for the inductor L, the input DC voltage V_c, the magnitude of tolerance band and the maximum implementation delays that could be tolerated, if the inverter bridge was to operate within a defined frequency band, for given values of output current I_s. The knowledge of these frequencies was essential to minimise switching losses, and for the design of the switching frequency current filter (Chapter 5).

c) the effect of implementation delays on the level of switching frequency current harmonics, using both unipolar and bipolar switching modes.

3.2. Theoretical Model

In a complex, non-linear, control system such as that of the utility connected PV inverter system shown in Figure 3.1, it is necessary to forecast performance characteristics based upon a simplified model before proceeding with its circuit design. The inverter bridge, the voltage and the current control loops and the AC filter shown as in Figure 3.1 form a 5^{th} order system, and the multiplier in the voltage control loop introduces some non-linearity. To carry out stability analyses of current and voltage controllers, they need to be linearised and simplified to manageable second order systems.

Issues related to interactions between the current loop and other control loops will be dealt with in later chapters. This approach will make it easier to identify and correct any likely sources of stability problems associated with the current loop circuits before adding the other control loops. Since the aim of this project is to minimise the power losses of the inverter, the maximum power tracker and the DC to DC converter will be considered as an ideal voltage source for modelling purposes.

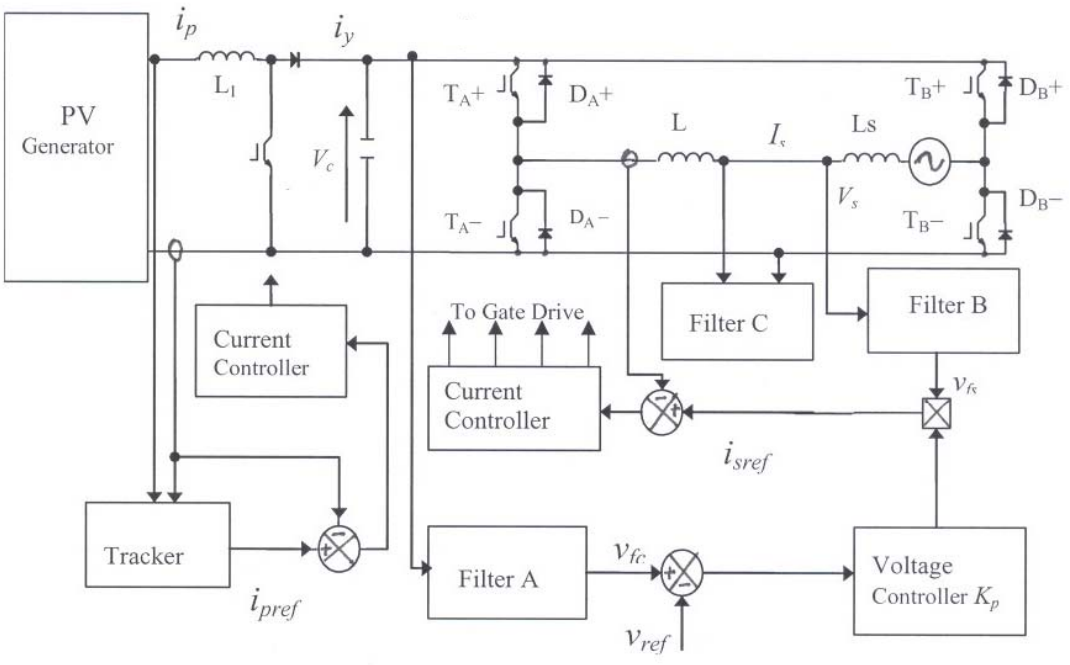


Figure 3.1: Utility connected PV system

The simplified mathematical model of the inverter current loop will be used to determine: -

- the relationship between the input DC voltage V_c, the mains supply voltage V_s, the magnitude tolerance band, and the inductance of inductor L required to achieve maximum efficiency.

- the effect of implementation delay on the level of current harmonics generated by both unipolar and bipolar switched inverters.

- the switching frequencies along the current waveform.

- the minimum switching frequency (F_{min}), which in turn determines the magnitude of the low frequency current harmonics.

- the maximum switching frequency (F_{max}) for the purpose of estimating switching losses.

The next phase of the theoretical design process was to use the dynamic system simulation package SIMULINK which is an extension of MATLAB [58, 59] to develop a model of the current loop. SIMULINK was chosen because of its speed and capability of simulating dynamic systems. The current loop parameters derived from the mathematical model were substituted in the SIMULINK model to determine the performance characteristics of the CCL and the magnitude of the current harmonics generated by the inverter.

3.3. Current Loop Design

The choice of switching frequencies is a trade off between switching losses, and the magnitude of current harmonics present in the inverter output. Both of these issues are of concern when designing the current control loop. If switching frequencies are

unknown, a designer may over-rate inverter components such as the power electronic switches, to avoid over stressing them during switching transients.

In applications where switching frequency filters are to be used, stability problems may occur if these switching frequencies coincide with the resonance frequency of the filter network. Failure to take such precautions may also lead to unacceptable levels of harmonic currents being injected into the grid supply. Therefore, the first step in current loop design is to determine the switching frequency variations over the current cycle using both the unipolar and the bipolar modes. Of particular interest are the switching frequencies near the peak, and also near the zero crossing of I_s, and in the case of the unipolar mode, the instantaneous value of I_s at which F_{max} occurred.

3.3.1. CCL Design Assumptions

Due to the large number of variables, to develop a simplified model of the CCL it was necessary to make the following assumptions: -

- the voltage control loop (VCL) was perfect (i.e. V_c was constant)
- the AC inductor L was ideal, stray capacitance and resistance were ignored
- the inverter electronic switches were perfect and therefore turn-on resistance was ignored
- the mains supply voltage V_s was a sinusoidal wave with a constant magnitude of 240V
- the inductance of the mains supply L_s was ignored as it was very much smaller than the AC inductor L
- the input DC voltage source was considered ideal, that is the 100 Hz ripple was ignored

- the effects of the PV array earth capacitance and any DC component of the inverter output current were ignored

- the loading effects of filters A and B were considered negligible.

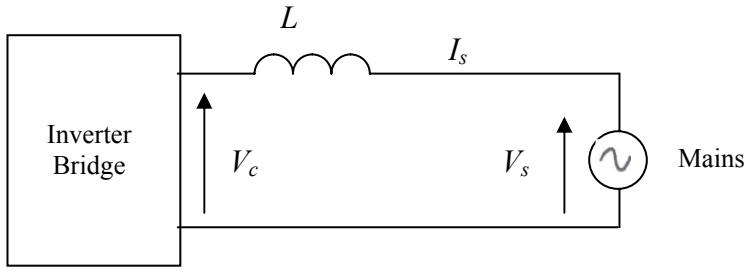


Figure 3.2: Simplified model of current control loop

Figure 3.3 shows the rise and fall of the switched current between the upper and lower limits of the hysteretic band. Since the inverter output current changes very slowly (50 Hz) with respect to the ripple current frequency (in the kHz range) the tolerance band limits are assumed to be straight lines.

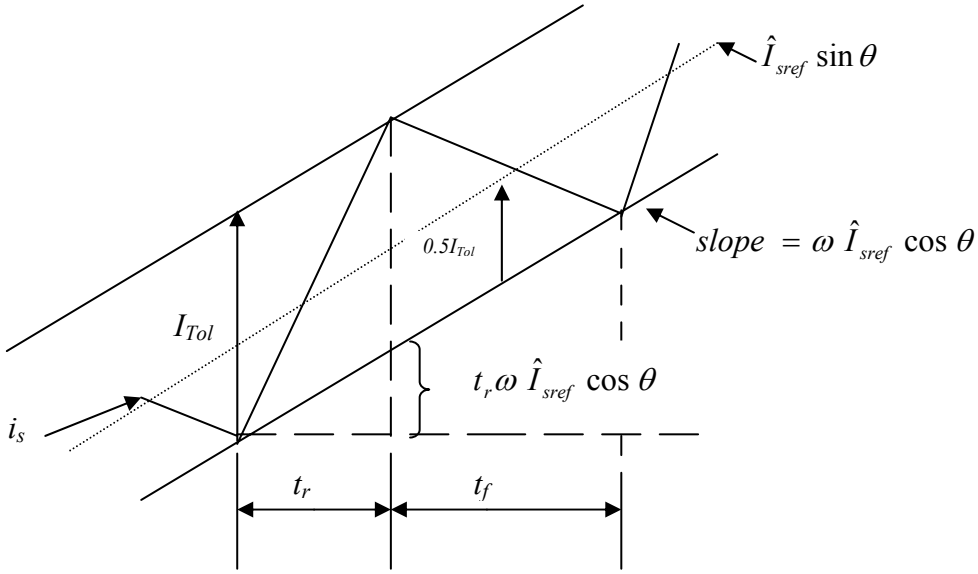


Figure 3.3: Hysteretic band current control (without circuit delay)

As mentioned in Chapter 1, in this project the hysteretic or tolerance band method is being used to control the maximum switching frequency (F_{max}). The switching frequency, which varies over a cycle using the tolerance band method, is a function of the magnitude of the tolerance band I_{Tol}, the total inductance L of the current loop, the voltage across L and the current I_s (Figure 3.2).

In this subsection, the emphasis is on estimating the switching frequency of the inverter using both bipolar and unipolar switching methods. For reasons of simplicity, the effects of circuit delay will not included in this subsection but will be incorporated in the next subsection.

3.3.2. Unipolar Operation without Circuit Delay

The design analysis to be presented in this and subsequent sections up to section 3.9, is an expanded version of a paper presented by Sharma at AUPEC 2001 [60].

With reference to Figure 3.2, the voltage across the inductor L when the current is increasing, is determined by equation 3.1.

$$L\frac{\Delta i_s}{\Delta t} = V_c - \hat{V}_s \sin\theta \tag{3.1}$$

From Figure 3.3:

$$\Delta i_s = I_{Tol} + t_r \omega \hat{I}_{sref} \cos\theta \tag{3.2}$$

The current rise time t_r of each switching cycle can be obtained using equation 3.3, which has been developed using equations 3.1 and 3.2, and replacing Δt by t_r.

$$t_r = \left[\frac{L\, I_{Tol}}{V_c - \hat{V}_s \sin\theta - \omega L\ \hat{I}_{sref} \cos\theta}\right] \tag{3.3}$$

Similarly, during intervals when the inductor current is diminishing, the current fall time t_f of each switching cycle can be obtained using equations 3.4 and 3.5.

$$L\ \frac{\Delta i_s}{\Delta t} = -\hat{V}_s \sin\theta \tag{3.4}$$

$$\Delta i_s = -(I_{Tol} - t_f \omega \hat{I}_{sref} \cos\theta) \tag{3.5}$$

$$t_f = \left[\frac{L\, I_{Tol}}{\hat{V}_s \sin\theta + \omega L\ \hat{I}_{sref} \cos\theta}\right] \tag{3.6}$$

Using equations 3.3 and 3.6 the switching frequency variation along the current waveform can be obtained:

$$F_s = \left[\frac{V_c \left\{ \hat{V}_s \sin\theta + \omega L \hat{I}_{sref} \cos\theta \right\} - \left\{ \hat{V}_s \sin\theta + \omega L \hat{I}_{sref} \cos\theta \right\}^2}{V_c L I_{Tol}} \right] \qquad (3.7)$$

By inspection:

At $\theta = 0^o$, $$F_0 = \frac{\omega L \hat{I}_{sref} \left[V_c - \omega L \hat{I}_{sref} \right]}{V_c L I_{Tol}} = \mathrm{F_{min}} \qquad (3.8)$$

$$\mathrm{F_{min}} \approx \frac{\omega \hat{I}_{sref}}{I_{Tol}} \qquad \text{if } \omega L \hat{I}_{sref} << V_c \qquad (3.9)$$

At $\theta = 90^o$, $$\mathrm{F_{90}} = \frac{\hat{V}_s \left(V_c - \hat{V}_s \right)}{V_c L I_{Tol}} = \mathrm{F_{med}} \qquad (3.10)$$

Finally, the maximum switching frequency ($\mathrm{F_{max}}$) can be found by differentiating equation 3.7 and setting $\frac{dF_s}{d\theta} = 0$, to give equation 3.11.

$$\mathrm{F_{max}} = \frac{V_c}{4L I_{Tol}} \qquad (3.11)$$

Since $\hat{V}_s$ is assumed constant at 340 V (supply voltage V_s =240 V), the switching frequency variations become a function of L, V_c, I_{Tol} and the inverter output current I_s where $I_s \approx I_{sref}$.

Equation 3.9 illustrates that for unipolar switching, as the current approaches zero, V_c and V_s have insignificant influence on the switching frequency. Since $\mathrm{F_{min}}$ is

governed by the magnitude of the tolerance band and the value of current I_s, the level of current distortion near the zero crossing may be of concern in the PV application where the current varies significantly throughout the day.

The switching frequency (F_{med}) at peak value ($\theta = 90^O$) of the current waveform, given by equation 3.10, is a useful frequency for estimating switching losses.

Equation 3.11 shows that the AC supply voltage V_s has no effect on the value of F_{max}.

3.3.3. Bipolar Operation without Circuit Delay

For bipolar switching the process is simpler, only the fall time t_f of the current is different. Therefore, the current rise time t_r is again given by equation 3.3. Also equation 3.5 for Δi_s is still applicable.

$$L\frac{\Delta i_s}{\Delta t} = -V_c - \hat{V}_s \sin\theta \tag{3.12}$$

Replacing Δt by t_f in equation 3.12 and using equation 3.5:

$$t_f = \left[\frac{L\, I_{Tol}}{V_c + \hat{V}_s \sin\theta + \omega L\ \hat{I}_{sref} \cos\theta}\right] \tag{3.13}$$

Equations 3.5 and 3.13 are used to derive equation 3.14.

$$F_s = \left[\frac{V_c^2 - \left\{\hat{V}_s \sin\theta + \omega L \hat{I}_{sref} \cos\theta\right\}^2}{2 V_c L I_{Tol}}\right] \tag{3.14}$$

Equation 3.14 can be used to determine F_{max} and F_{min}.

When $\theta = 0^o$:

$$F_0 = \frac{V_c^2 - \left(\omega L \hat{I}_{sref}\right)^2}{2V_c L I_{Tol}} \tag{3.15}$$

By differentiating equation 3.14,

$$F_{max} = \frac{V_c}{2L I_{Tol}} \tag{3.16}$$

When $\theta = 90^o$:

$$F_{90} = \frac{V_c^2 - \hat{V}_s^2}{2V_c L I_{Tol}} = Fmin \tag{3.17}$$

As expected, the simplified equations 3.11 and 3.16 show that theoretically, if the same values of L, V_c and I_{Tol} are used for the two switching modes, then F_{max} is twice using bipolar switching when compared to unipolar switching. Therefore, as stated in Chapter 2, theoretically (if delay is ignored) for a given F_{max}, half the value of inductance is required (less copper therefore lower power losses) in the unipolar mode compared to the bipolar mode, if hysteretic current control is used.

3.3.4. Numerical Calculations

For the purpose of estimating F_{min}, F_{med}, F_{max} and the switching frequency along the current waveform, reasonable values of V_c, L and I_{Tol} were chosen.

a) Since the voltage $\hat{V}_S$, is set by the power supply authorities, it was chosen to be 340 V.

b) Theoretically, to avoid distortion of the inverter output current reaching unacceptable levels, the minimum DC voltage V_c needs to be greater than $\hat{V}_S$ (340 V). However, if the legal limits of the mains supply voltage are taken into consideration then the minimum value of V_c needs to be greater than 358 V. Since all practical feedback control circuits will have some implementation circuit delays, the value chosen for V_c was 400 V.

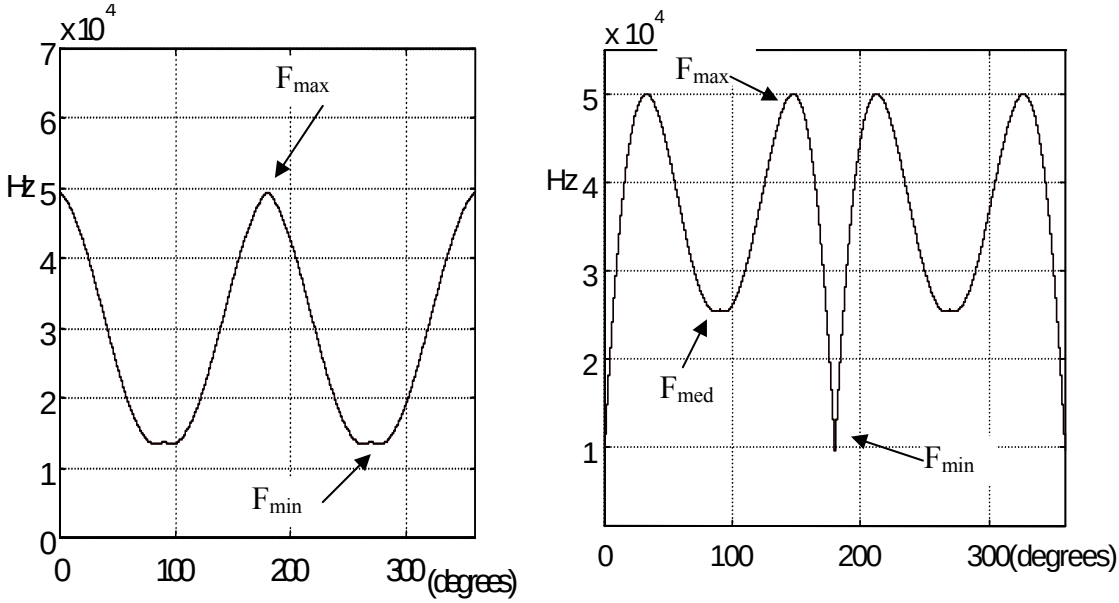
c) To minimise the current distortion at the zero crossing and to make the phase difference between V_s and I_s as small as possible, the inductance L chosen for bipolar switching was 20 mH and for unipolar switching, was 10 mH. Theoretically, using equations 3.11 and 3.16 should yield the same value for F_{max} for the both switching modes.

d) To achieve a reasonable switching frequency, the tolerance band, I_{Tol} was initially chosen as 0.2 A.

e) Since a 1 kW PV system is being considered, the rated current is used as the value of I_s ($\hat{I}_s = \hat{I}_{sref}$ = 5.9 A and ω = 314 rad/s).

Table 3.1: Switching Frequency comparison for unipolar and bipolar mode

Frequency	Unipolar Switching	Bipolar Switching
F_{max}	50 kHz	50 kHz
F_{med}	25.5 kHz	
F_{min}	9.3 kHz	13.9 kHz



(a) Bipolar Switching (b) Unipolar Switching

Figure 3.4: Switching frequency variation along current waveform

The following conclusions can be made from these simulation results: -

a) As expected, (equations 3.11 and 3.16), if twice the value of inductance *L* is used in the bipolar mode compared to the unipolar mode (all other current loop parameters kept the same) the magnitude of F_{max} is the same (Table 3.1).

b) In the unipolar mode, knowledge of the switching frequency F_{med} at the peak value of the current I_s is important because the switching frequency harmonics lie between Fmed and Fmax for about 90% of the current cycle (Figure 3.4

(b)). This information will assist inverter designers in estimating switching losses and hence the size of heat sinks required for the inverter switches.

c) In the unipolar mode, as the current I_s approaches the zero crossing, F_{min} may be of some concern because the switching frequency becomes solely a function of the magnitude of the tolerance band I_{Tol} and the inverter output current I_s (equation 3.9). The significance of this result is that distortion problems near the current zero crossing in a unipolar switched inverter may be much greater when it is operating well below its rated current. This could be of concern in the proposed PV application in this project.

d) An advantage of unipolar switching is that at the peak value of the output current I_s, the switching frequency F_{med} is almost twice that in bipolar. This result indicates that the potential distortion of the current at its peak due to lower switching frequency is greater in the bipolar mode.

It should be pointed out that these theoretical results were obtained to verify the important relationship between unipolar and bipolar switching in an ideal situation (without delay) and should be kept in proper perspective.

3.4. Switching Frequency Changes due to Delay

Implementation delays (t_d) such as blanking time, dead time and unwanted propagation delays are unavoidable when designing practical current control loops, and have been discussed in Chapter 2. Changes in switching frequency due to implementation delays will be investigated for the unipolar and bipolar modes in this subsection.

3.4.1. Unipolar Switching

When using the hysteretic current technique, these delays have the same effect as increasing the width of the tolerance band I_{Tol}. This equivalent increase in I_{Tol} due to t_d can be determined by using Figure 3.5 as $(\Delta i_L + \Delta i_u)$.

Where $\Delta i_u = t_d$ [slope of current ramp – slope of I_{sref}] and

$\Delta i_L = t_d$ [slope of I_{sref} - slope of current ramp]

Hence $\Delta i_u + \Delta i_L = \frac{t_d}{L}\left[V_c - \hat{V}_s \sin\theta + \hat{V}_s \sin\theta\right]$

$$\Delta i_u + \Delta i_L = \frac{t_d V_c}{L} \tag{3.18}$$

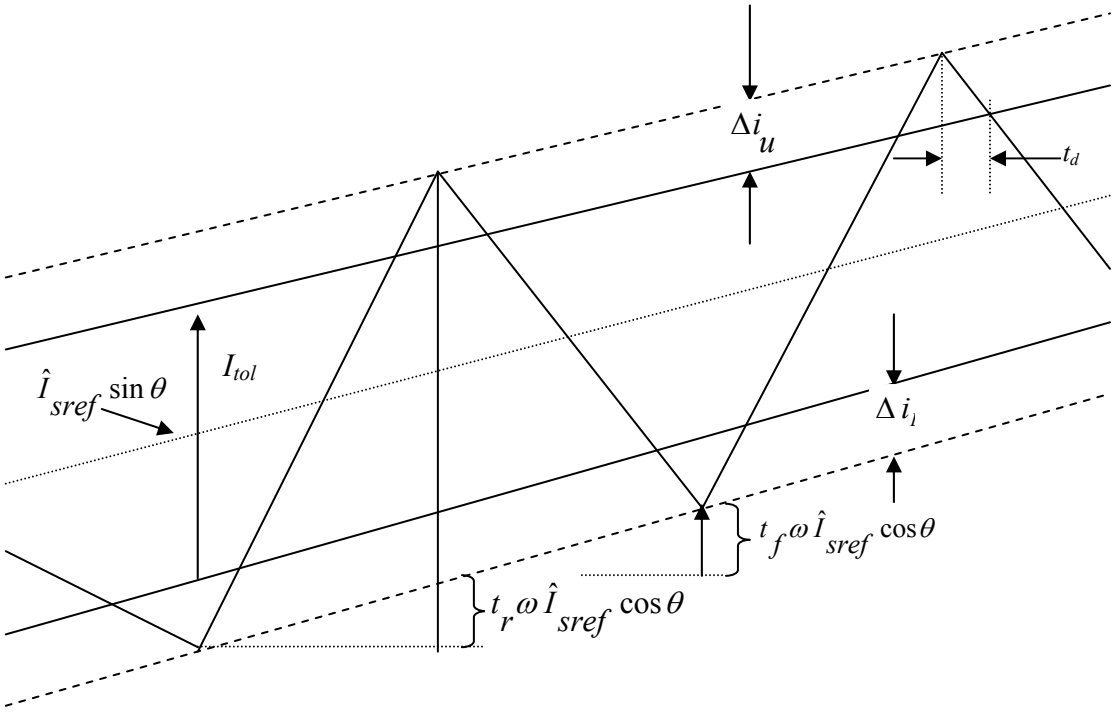


Figure 3.5: Hysteretic band current control (with circuit delay)

When the instantaneous current is increasing, using equation 3.18 and Figure 3.5:

$$\Delta i_s = I_{Tol} + \Delta i_L + \Delta i_u + t_r \omega \hat{I}_{sref} \cos\theta$$

$$\Delta i_s = I_{Tol} + \frac{t_d V_c}{L} + t_r \omega \hat{I}_{sref} \cos\theta \tag{3.19}$$

Using equation 3.1 and 3.19 the current rise time t_r during each switching cycle can be determined (equation 3.20).

$$t_r = \left[\frac{L\ I_{Tol} + t_d V_c}{V_c - \hat{V}_s \sin\theta - \omega L\ \hat{I}_{sref} \cos\theta} \right] \tag{3.20}$$

Similarly:

$$\Delta i_s = -\left[I_{Tol} + \frac{t_d V_c}{L} - t_f \omega \hat{I}_{sref} \cos\theta \right] \tag{3.21}$$

Using equations 3.4 and 3.21, the current fall time t_f for each switching cycle can be determined (equation 3.22).

$$t_f = \left[\frac{L\ I_{Tol} + t_d V_c}{\hat{V}_s \sin\theta + \omega L\ \hat{I}_{sref} \cos\theta} \right] \tag{3.22}$$

To minimise distortion, the tolerance band is small compared to the rated current and hence it can be assumed that $\hat{I}_s \approx \hat{I}_{sref}$. Therefore equation 3.23 can be obtained using equations 3.20 and 3.22. Equation 3.23 a new theoretical description of the switching frequency variations along the current waveform for hysteretic current control unipolar switched inverters that include implementation delay.

$$F_s = \left[\frac{L\ I_{Tol} + V_c\ t_d}{V_c - \hat{V}_s \sin\theta - \omega L\ \hat{I}_s \cos\theta} + \frac{L\ I_{Tol} + V_c\ t_d}{\hat{V}_s \sin\theta + \omega L\ \hat{I}_s \cos\theta} \right]^{-1} \tag{3.23}$$

Equation 3.23 can be simplified to give equations 3.24 to 3.26 to allow estimation of important switching frequencies that will assist in the design of the current loop to be estimated.

when $\theta = 0^o$ and if $\omega L \hat{I}_{sref} << V_c$:

$$F_{min} = \frac{L\ \omega \hat{I}_s}{L\ I_{Tol} + V_c t_d} \tag{3.24}$$

When $\theta = 90^o$:

$$F_{med} = \frac{\hat{V}_s \left(V_c - \hat{V}_s\right)}{V_c \left(L\, I_{Tol} + V_c t_d\right)} \tag{3.25}$$

Finally, the maximum switching frequency can be found by differentiating equation 23 and equating the derivative to zero:

$$F_{max} = \frac{V_c}{4(L\ I_{Tol} + V_c t_d)} \tag{3.26}$$

3.4.2 Bipolar Switching

If implementation delays are included in the bipolar case then the current rise time t_r (equation 3.29) during each switching cycle can be obtained using equations 3.1, 3.27 and 3.28.

Again, using the same method as in the unipolar case, and using Figure 3.5 and equations 3.1 and 3.12:

$$\Delta i_u + \Delta i_L = \frac{t_d}{L}\left[V_c - \hat{V}_s \sin\theta + V_c + \hat{V}_s \sin\theta\right]$$

$$\Delta i_u + \Delta i_L = \frac{2 t_d V_c}{L} \tag{3.27}$$

$$\Delta i_s = I_{Tol} + \frac{2 t_d V_c}{L} + t_r \omega \hat{I}_{sref} \cos\theta \tag{3.28}$$

$$t_r = \left[\frac{L\, I_{Tol} + 2\, t_d V_c}{V_c - \hat{V}_s \sin\theta - \omega L\ \hat{I}_{sref} \cos\theta} \right] \tag{3.29}$$

Similarly, using equations 3.12 and 3.30, the current fall time t_f for each switching cycle and hence the switching frequency along the current waveform can be determined (equation 3.32).

$$\Delta i_s = -\left[I_{Tol} + \frac{2\, t_d V_c}{L} - t_f \omega \hat{I}_{sref} \cos\theta \right] \tag{3.30}$$

$$t_f = \left[\frac{L\, I_{Tol} + 2\, t_d V_c}{V_c + \hat{V}_s \sin\theta + \omega L\ \hat{I}_{sref} \cos\theta} \right] \tag{3.31}$$

$$F_s = \left[\frac{L\ I_{Tol} + 2 V_c\, t_d}{V_c - \hat{V}_s \sin\theta - \omega L\ \hat{I}_s \cos\theta} + \frac{L\ I_{Tol} + 2 V_c\, t_d}{Vc + \hat{V}_s \sin\theta + \omega L\ \hat{I}_s \cos\theta} \right]^{-1} \tag{3.32}$$

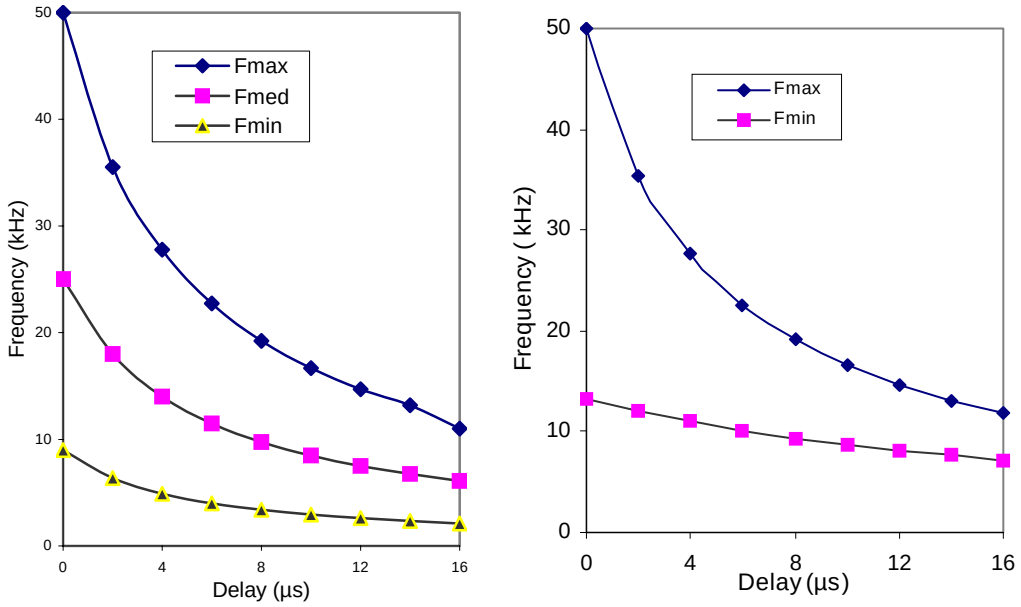
By substituting 0^o and 90^o for θ in equation 3.32, F_{max} and F_{min} can be estimated using equations 3.33 and 3.34.

$$F_{min} \approx \frac{\left(V_c^2 - \hat{V}_s^2 \right)}{2 V_c \left(L\, I_{Tol} + 2 V_c t_d \right)} \tag{3.33}$$

$$F_{max} \approx \frac{V_c}{2(L I_{tol} + 2 V_c t_d)} \tag{3.34}$$

Numerical solutions using equations 3.23 and 3.32, shown in Figure 3.6, illustrate that circuit delays have greater effect on the switching frequency if the unipolar mode is used compared to the bipolar mode. Using the same system parameters as in section 3.3.4, in the case of bipolar, F_{min} fell by 46% (occurs at the peak value of

current) while in the unipolar mode F_{min} decreased by 78% (occurs near the current zero crossing) when delay was increased from zero to 16µs. It is therefore important that implementation delays are included in the design procedures for unipolar switched inverters. The simplified equations 3.24 and 3.33 are simple tools that can be used by inverter designers to prevent the switching frequency from falling below the value of 2 kHz suggested by Boys and Green [24].



(a) Unipolar Switching (b) Bipolar Switching

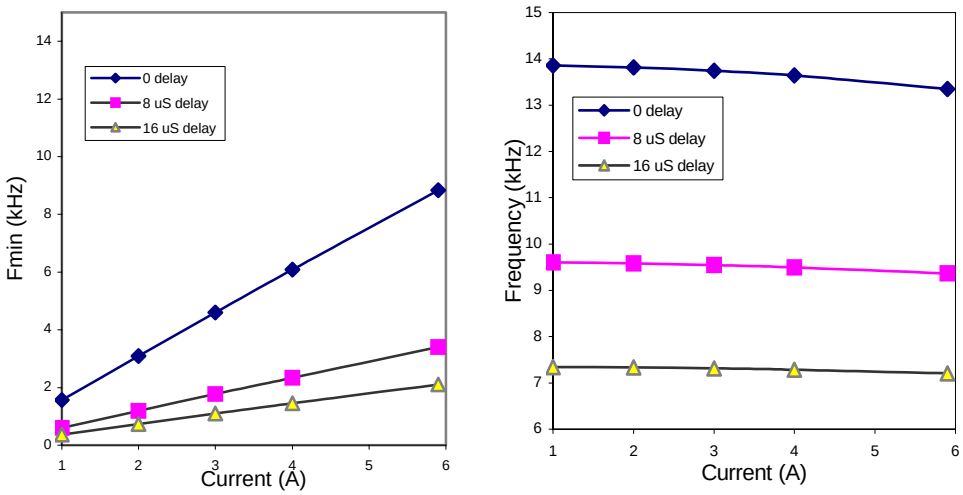
Figure 3.6: Effect of delay on switching frequency

For the unipolar mode, the value of F_{med} is useful because it allows a more realistic estimation of the average switching frequency and hence switching losses to be made. From Figure 3.4 it can be estimated that for over 90% of the inverter output current cycle, the switching frequency lies between F_{max} and F_{med}. Knowledge of these key frequencies is also useful when designing switching frequency filters.

In PV applications the current I_s continuously changes, and therefore in the next subsection the combined effect of current changes and circuit delays on F_{min} is presented.

3.5. Effect of Changes in I_S on F_{min}

In all the previous cases, current $\hat{I}_S$ was kept constant at its rated value. However in this section the current and the circuit delays are varied while all the current loop parameters for the two modes of switching are kept the same as in the previous cases. This exercise is important as the current $\hat{I}_S$ and hence $\hat{I}_{sref}$ ($\hat{I}_s \approx \hat{I}_{sref}$) is not at its maximum through the day.



a) Unipolar Switching b) Bipolar Switching

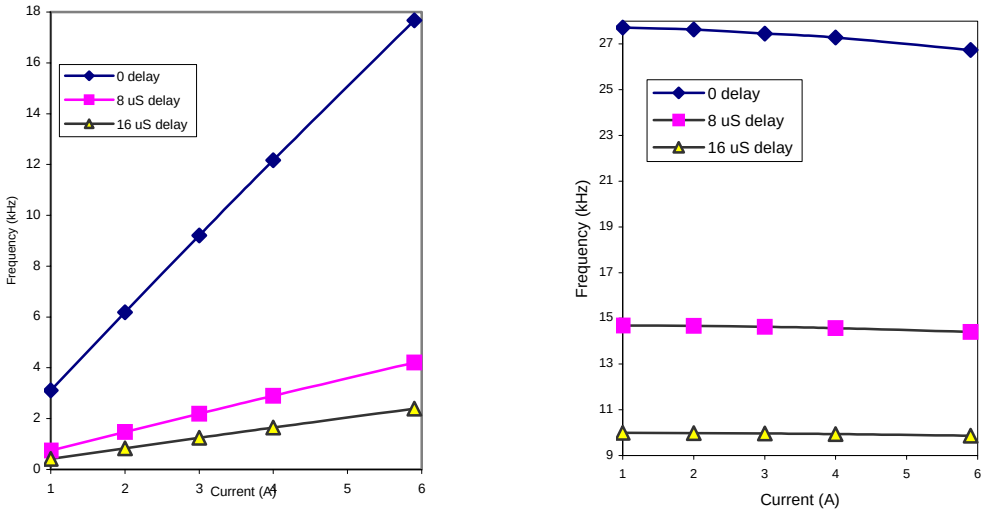
Figure 3.7: Combined effect of changes in I_s and delay on F_{min} (for I_{Tol} = 0.2 A)

The combined effect on F_{min} of varying the current $\hat{I}_S$ from 1 A to 5.9 A (peak value of inverter rated current) and the delay from 0 to 16 µs is shown in Figure 3.7. These results further indicate that when using unipolar switching, unacceptable magnitudes of current distortion may occur near the zero crossing if the implementation delay is greater than 8 µs and if the output current I_s falls below 50% of the rated value. Bipolar switching on the other hand has an advantage that F_{min} is less affected by the combined effect of circuit delay and current changes and remains well above 2 kHz.

The relationship between low frequency current harmonics and implementation delay will be examined in subsection 3.8.

3.6. Effect of Changing I_{Tol} on F_{min}

In the previous subsection the magnitude of the tolerance band I_{Tol} was kept constant at 0.2 A. The tests carried out in section 3.5 are repeated with all the control loop parameters unchanged except I_{Tol}, which is reduced by 50% to 0.01 A. The aim of this exercise is to establish if F_{min} can be increased significantly by using a tighter tolerance band.



a) Unipolar Switching b) Bipolar Switching

Figure 3.8: Effect of changes in I_s, and delay on F_{min} (for I_{Tol} = 0.1 A)

For 8 μs delay, comparison of Figures 3.7 and 3.8 show that there is an increase of about 20% in F_{min} in the unipolar mode, and about 30% in the bipolar mode. However, for the unipolar mode, reducing the magnitude of the tolerance band by 50% does not improve the value of F_{min} to above 2 kHz for values of $\hat{I}_S$ less than 3 A. To explain the reasons for this, consider the denominator of equation 3.24 ($L\ I_{Tol} + V_c\ t_d$). The circuit delay becomes dominant when $t_d > \frac{I_{Tol} L}{V_c}$. Substituting previous numerical values for L, I_{Tol} and V_c gives a value of 5 μs for t_d when the tolerance band is reduced from 0.2 A. That is, reducing the tolerance band becomes ineffective for circuit delays greater than 5 μs. This result also implies that a *variable tolerance band* as opposed to a fixed tolerance band (chosen in this project) may not solve potential distortion problems near the zero crossing.

This result also illustrates that while using unipolar switching leads to lower power losses [30], the minimum value of L is to a large extent governed by the total implementation delay, if unacceptable levels of current harmonics injected into the grid are to be avoided. Again, equation 3.24 can be used to show that as t_d increases, F_{min} decreases.

3.7 Effect of Changes in V_S on Switching Frequencies

The purpose of this exercise is to determine the magnitude of switching frequency variations due to changes in the mains supply voltage V_s. This test is necessary as variation in V_s may lead to distortion of the current around its peak value.

The effects of changes in V_s can be demonstrated using equations 3.23 for unipolar switching and 3.32 for bipolar switching. However, as shown by the simplified equations 3.25 and 3.33, changes in V_s will largely affect the switching frequencies at the peak value of the current I_s. Numerical results with a variation of ±6% in $\hat{V}_S$, with all other parameters of the current loop kept the same as in section 3.5.1 are shown in Table 3.2.

Table 3.2: Effect of changes in $\hat{V}_S$ on switching frequency at $\hat{I}_S$

$\hat{V}_S$	F_{med} (Unipolar)	F_{min} (Bipolar)
320V	32 kHz	17.5 kHz
340V	25 kHz	13.4 kHz
360V	17.9 kHz	9.89 kHz

In the unipolar mode, changes of $\hat{V}_S$ ±20 V produced a change of 28% in the value of F_{med} while similar changes in V_s in the bipolar mode resulted in a change of 26% (360V) and 30.4% (320 V) in the value of F_{min}.

Knowledge of the switching frequencies is useful to estimate switching losses, and to help inverter designers make better choices of current loop components. However, for unipolar switched inverters to be a viable option, the magnitude of harmonic currents harmonics injected into the grid system must satisfy Australian Standards [4]. Therefore, in the next subsection, theoretical SIMULINK models will be developed to estimate the levels of current harmonics generated by the CCL using the unipolar and bipolar modes.

3.8. Current Harmonics using Bipolar Operation with no Delay

Current harmonics from grid connected energy systems via inverters must not exceed the limits specified in Table 3.3. These current harmonic limits are specified for the inverter AC output operating in the range 100±5% of its rated output [4]. Therefore to satisfy these limits the proposed inverter system needs to be tested at its rated output.

Table 3.3: Current harmonic limits (From AS4777.2, 2005 section 4.5)

Harmonic Order	Limit for each individual harmonic as a percentage of fundamental
2-9	4%
10-15	2%
16-21	1.5%
22-33	0.6%
Even harmonics	25% of equivalent odd harmonic
THD (to 50^{th} harmonic)	5%

The operational behaviour of the current loop using the bipolar mode can be described by the differential equation 3.35. As the inverter in this project is to be used only in the converter mode, its rectifying configuration is ignored.

$$\frac{di_s}{dt} = \frac{\left(SV_c - \hat{V}_s \sin\theta\right)}{L} \tag{3.35}$$

where $S = 1$ if T_{A+} and T_{B-} are on to increase the current I_s and

$S = -1$ if T_{A-} and T_{B+} are on to decrease the current I_s.

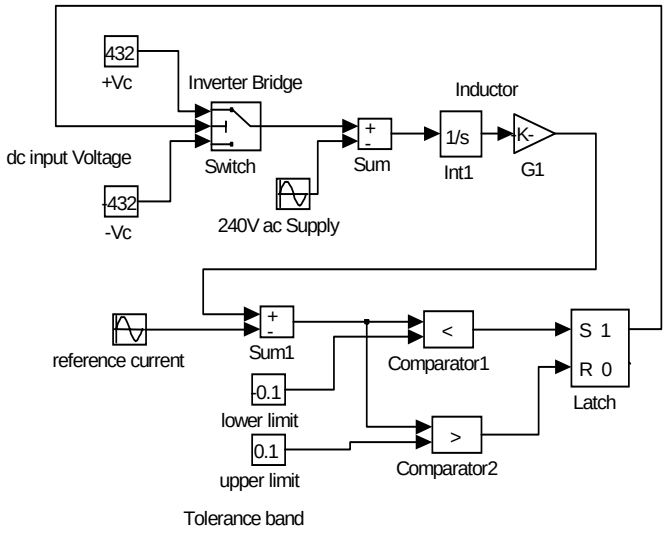
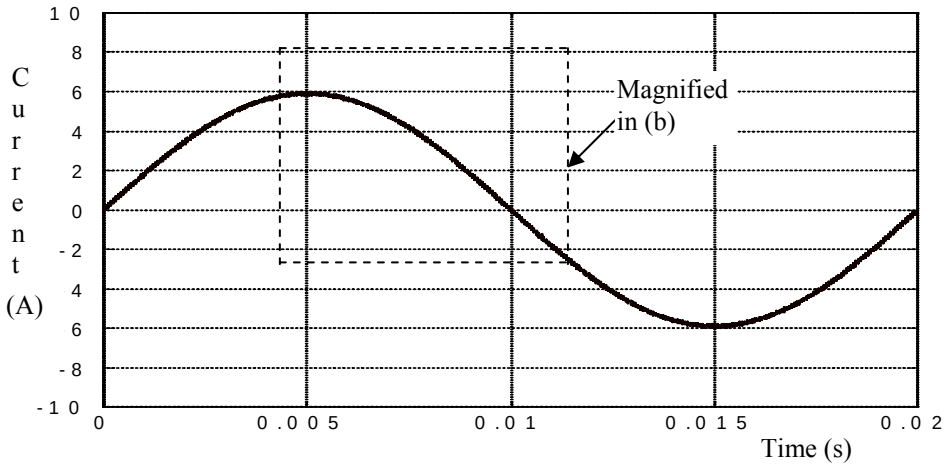


Figure 3.9: SIMULINK model of CCL (bipolar switching)

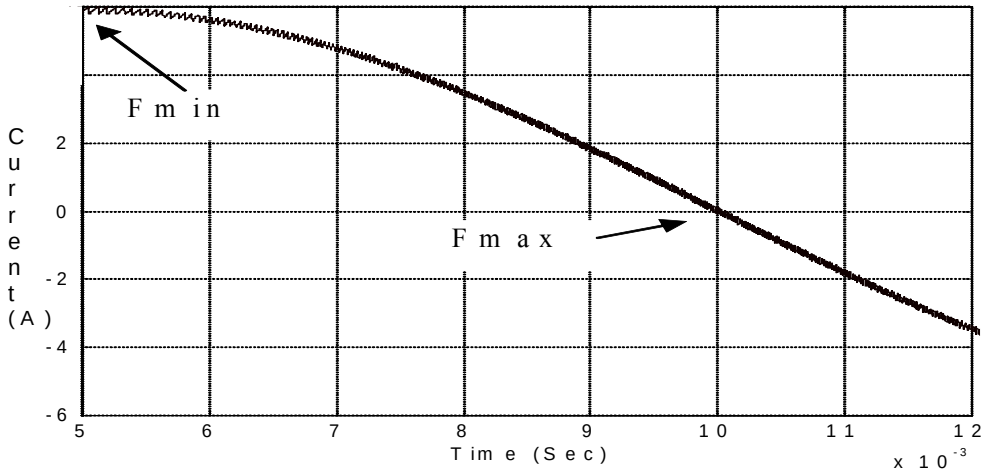
The SIMULINK model of the current loop model for bipolar switching shown in Figure 3.9 is produced using equation 3.35. Comparators 1, 2 and the RS latch represent the current controller whose function is to force the inductor current to stay within a fixed tolerance band around a reference current.

To simulate the current control loop, the values chosen for V_c, V_s, I_s t_b and L were the same as those used to estimate the switching frequencies in the previous subsections.

A discrete Fourier transform of the inverter output current i_s was carried out using MATLAB's inbuilt Fast Fourier Transform (FFT) function to estimate the magnitude of switching frequency current harmonics. The simulation results of the level of switching frequency harmonics (without implementation delay) are shown in Figures 3.10 and 3.11.

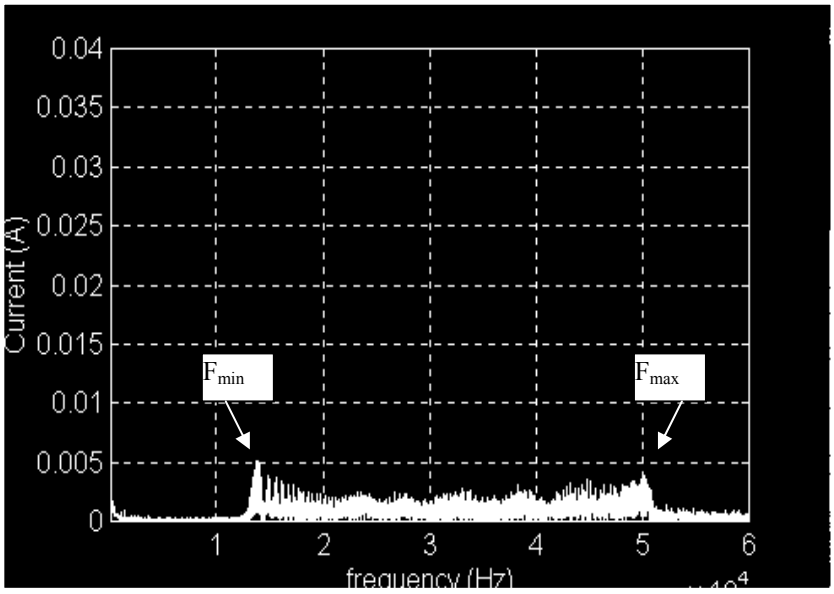


a) Inverter output current

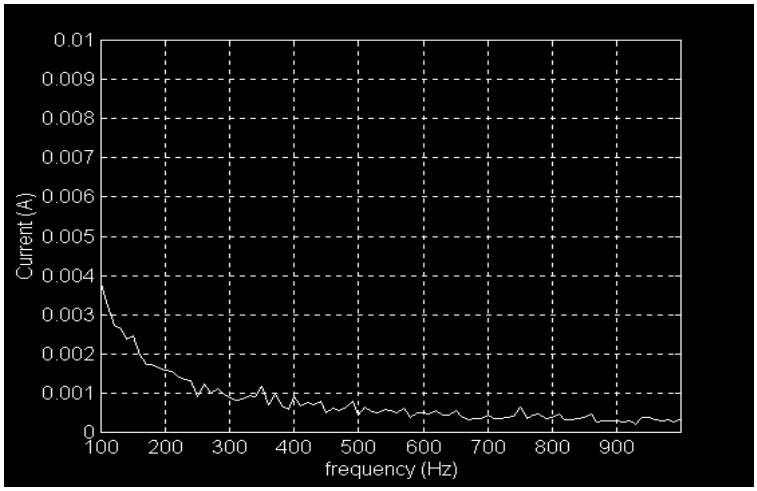


b) Magnified view showing maximum and minimum switching frequencies

Figure 3.10: Inverter output current using bipolar switching



a) Bipolar: Low and medium frequency harmonics



b) Bipolar: Low frequency harmonics

Figure 3.11: Frequency spectrum of i_s

The results for bipolar switching frequencies using SIMULINK agree with the results obtained using the analytical method, for F_{min} and F_{max} of 13.875 kHz and 50 kHz respectively, as given in Table 3.1.

The frequency spectrum of the current i_s shows that the maximum level of low switching frequency harmonics at rated inverter output was negligible. For example, the simulation result for the 3rd harmonic was 0.64 % which was very small compared to the 4.0 % limit shown in Table 3.3. The absence of low frequency harmonics indicates that for zero circuit delays, the output from bipolar switched inverters is effectively sinusoidal.

3.9. Current Harmonics using Unipolar Operation with no Delay

In unipolar switching, the operational behaviour of the current loop can be described by the same differential equation 3.35 used for bipolar. However, the variable *S*, which describes the switching functions, is different and is as follows: -

$S = 1$ if T_{A+} and T_{B-} are on

$S = -1$ if T_{A-} and T_{B+} are on

$S = 0$ if T_{A+} and D_{B+} are on *or* if D_{A+} and T_{B+} are on; alternatively

$S = 0$ if D_{A-} and T_{B-} are on *or* if T_{A-} and D_{B-} are on

To simulate the current controller using unipolar switching, apart from the value of *L* (10 mH), all other parameters chosen were the same as those used for bipolar mode. Figure 3.12 shows the SIMULINK model of the unipolar switched current loop. Again, a discrete Fourier transform of i_s was carried out and the simulation results are shown in Figures 3.13 and 3.14.

The frequency spectrum of the current i_s shows that the levels of harmonics at low frequencies and harmonics at switching frequencies were negligible. Again, the absence of low frequency harmonics for zero circuit delays indicates that the output current from unipolar switched inverters is effectively sinusoidal.

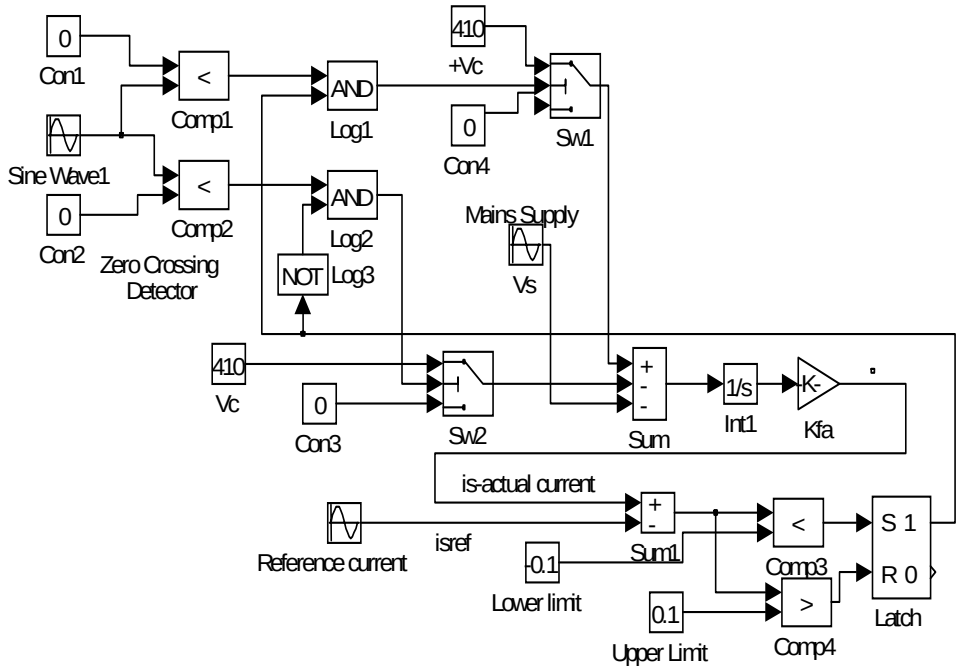


Figure 3.12: SIMULINK model of CCL (unipolar switching)

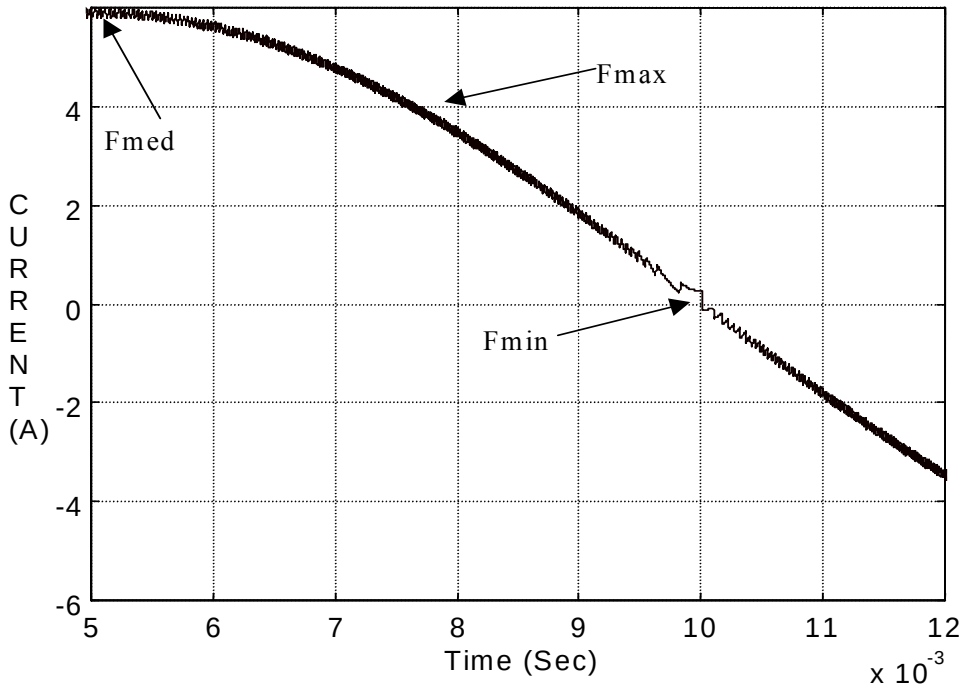
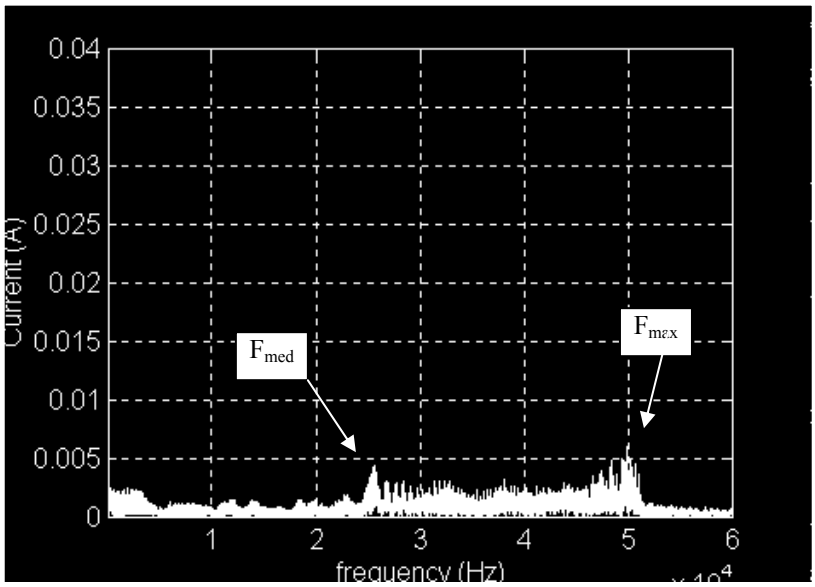
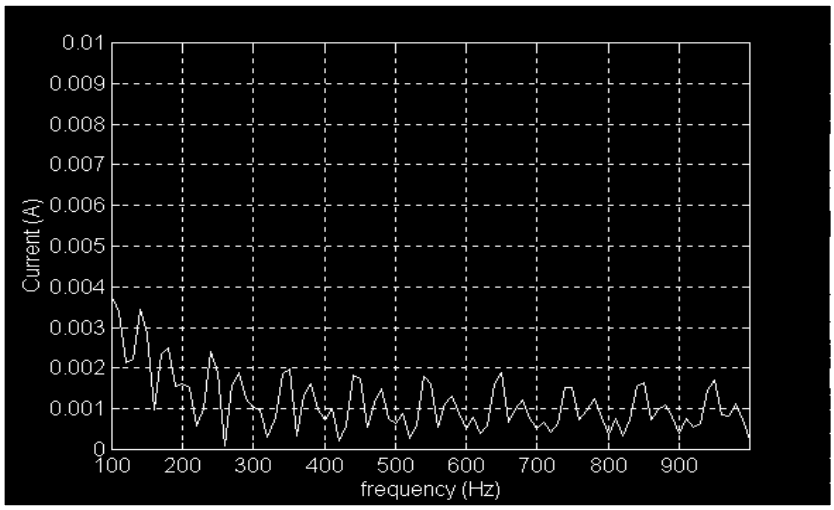


Figure 3.13: Inverter Output Current using unipolar switching



(a) Unipolar: low and medium frequency harmonics



(b) Unipolar: low frequency harmonics

Figure 3.14: Frequency spectrum of i_s (unipolar switching)

The results for unipolar switching using SIMULINK agree with the results obtained using the analytical method, for F_{med} and F_{max} of 25.5 kHz and 50 kHz respectively, as given in Table 3.1.

It has been stated by Itoh [61] that PWM current control can generate near sinusoidal current that leads to decreases in losses and magnetic noise, which with unity power factor contributes to minimisation of supply transformer rating. The results obtained in this section for the PWM unipolar and bipolar switched inverters, with zero implementation delay, support the work published by Itoh [61]. However, it will be shown in the next section that PWM current control will not generate sinusoidal current for non-zero implementation delay.

3.10. Effect of Delay on Harmonic Currents

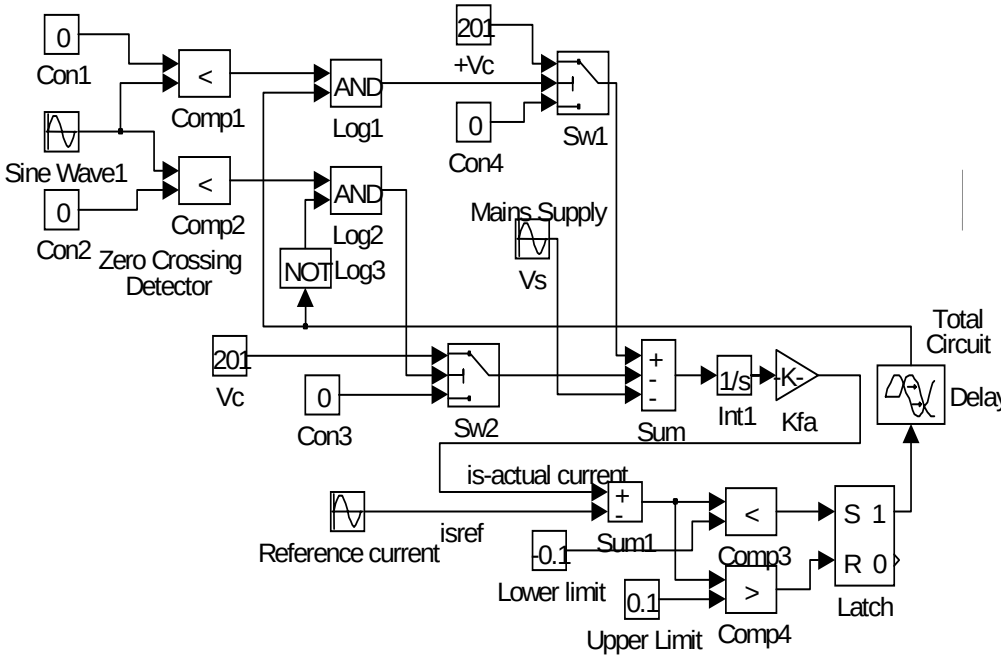


Figure 3.15 SIMULINK model of CCL (unipolar switching with delay)

To reach a more meaningful conclusion regarding the level of current harmonics generated by unipolar and bipolar switched inverters, the effect of circuit delays will be investigated in this subsection. For convenience, all the delays have been lumped together as shown in Figure 3.15 (unipolar mode) and Figure 3.16 (bipolar mode). In practice, the effects of intentional (eg blanking time and dead time) and unintentional delays (eg circuit propagation delays) on the current controller may be different at

different parts of the circuit. For example, all the four gate drive circuits may not necessarily have exactly the same propagation delays and as such the theoretical results should be kept in proper perspective. Despite this, the simulation exercise with delay included should provide a useful relationship between delay and level of current harmonics generated by unipolar and bipolar switched inverters.

Simulated output current spectra for a delay of 4 μs are shown in Figures 3.17 and 3.18, for unipolar and bipolar operations respectively. For the tolerance band to be effective (subsection 3.6), a delay of less than 5 μs had to be chosen. Hence, an implementation delay of 4 μs was chosen.

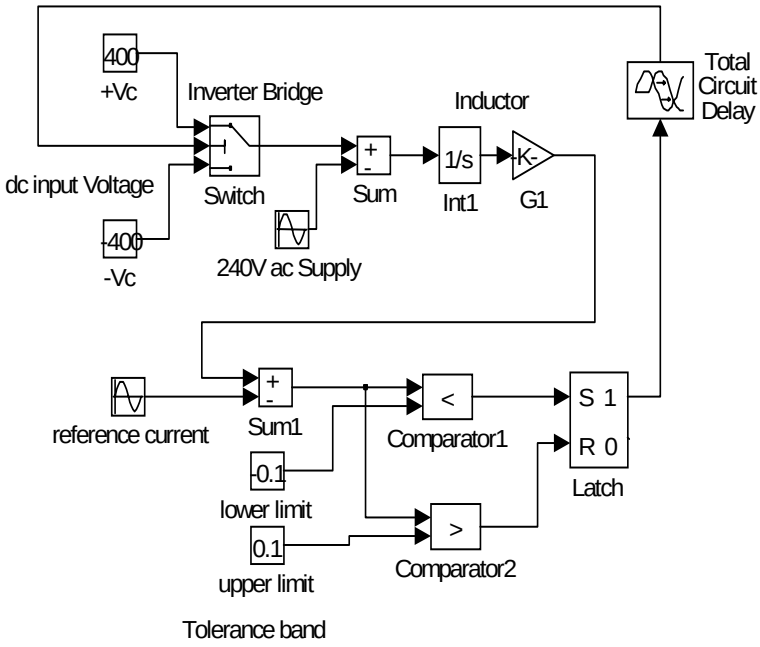
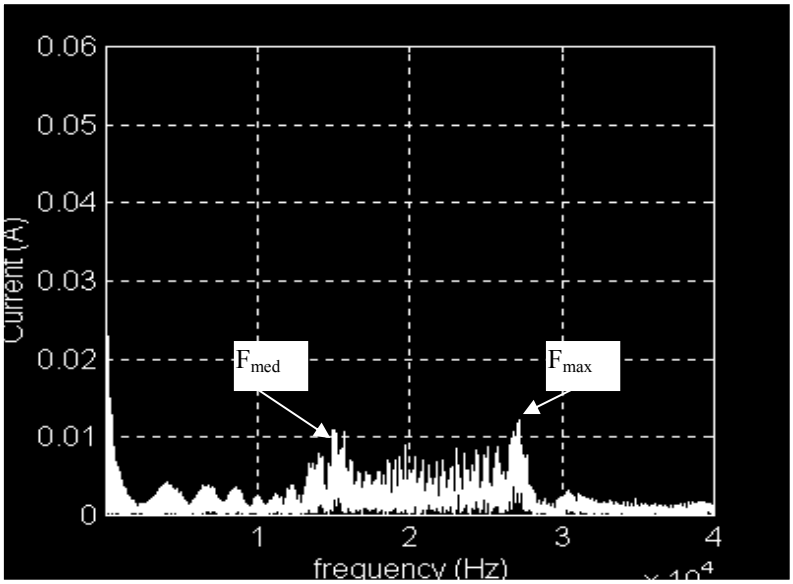
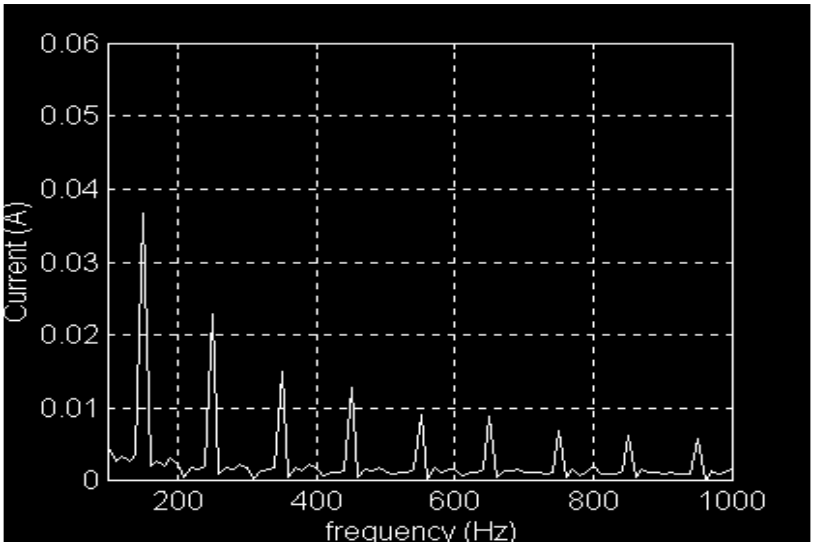


Figure 3.16 SIMULINK model of CCL (bipolar switching with delay)



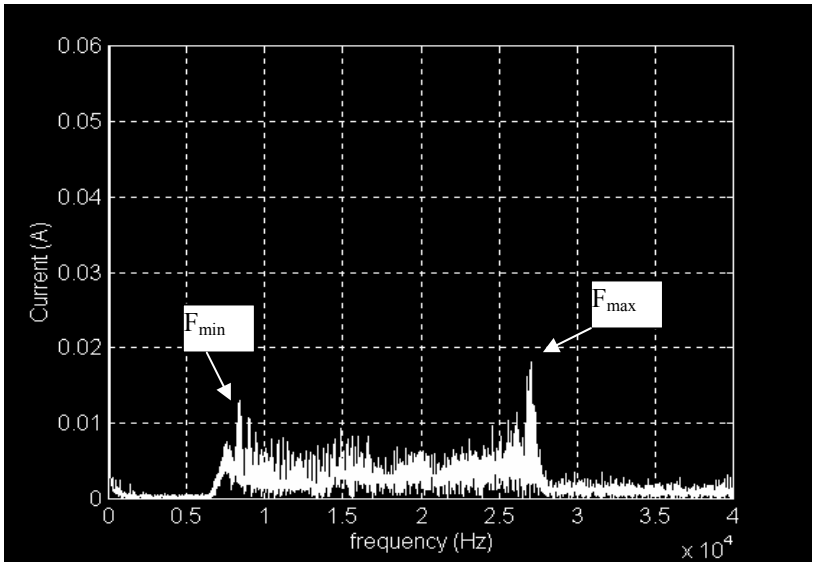
(a) Switching frequency current harmonic spectrum (unipolar)



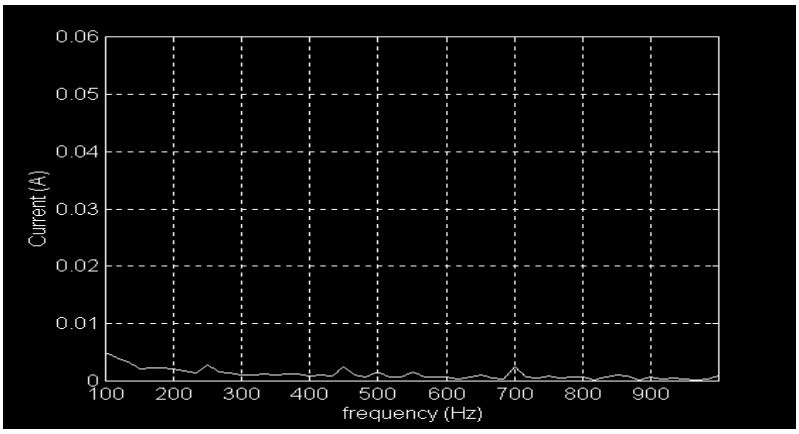
(b) Low frequency current harmonics (unipolar)

Figure 3.17: Unipolar switching current spectra with 4μs implementation delay, at rated output current of 4 A

For unipolar switching, the values of F_{med} and F_{max} from FFT of the current using SIMULINK, agree with the numerical results (F_{med} =14.12 kHz and F_{max} = 27.78 kHz) given in Figure 3.6 (a).



(a) Switching frequency harmonic spectrum (bipolar)



(b) low frequency Current harmonics (bipolar)

Figure 3.18: Bipolar switching current spectra with 4μs implementation delay included, at rated output current of 4 A

For bipolar switching, the values of F_{min} and F_{max} from FFT of the current using SIMULINK, also agree with the numerical results shown in Figure 3.6 (b).

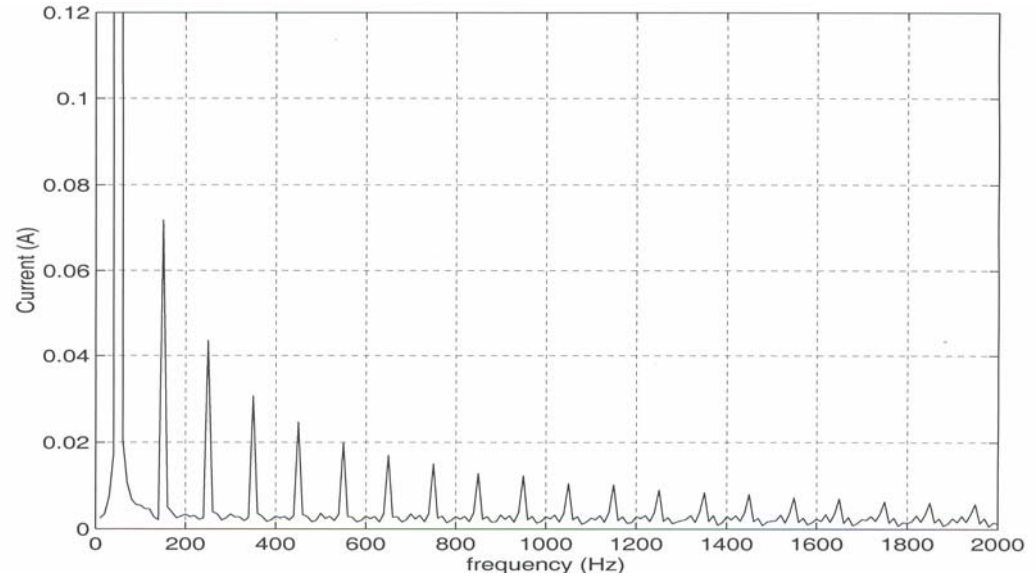
The harmonic analysis of the unipolar switched inverter rated output current reveals simulation significant increase in the levels of low frequency harmonics. For an example, the 3rd harmonic current increases from about 0.09% for zero delay to about 0.64% for an implementation delay of 4μs. They are however, practically non-

existent in the case of the bipolar switched inverter (Figures 3.17 (b) and 3.18 (b)). On the other hand, as the switching delay increases, the switching frequency harmonics generated by the bipolar switched inverter increases faster than those of the unipolar switched inverter (Figures 3.17 (a) and 3.18 (a)). For an example, when the delay was increased from zero to 4μs, the switching frequency harmonics at F_{max} for unipolar and bipolar modes increased from 0.15% to 0.2%, and 0.07% to 0.32% respectively.

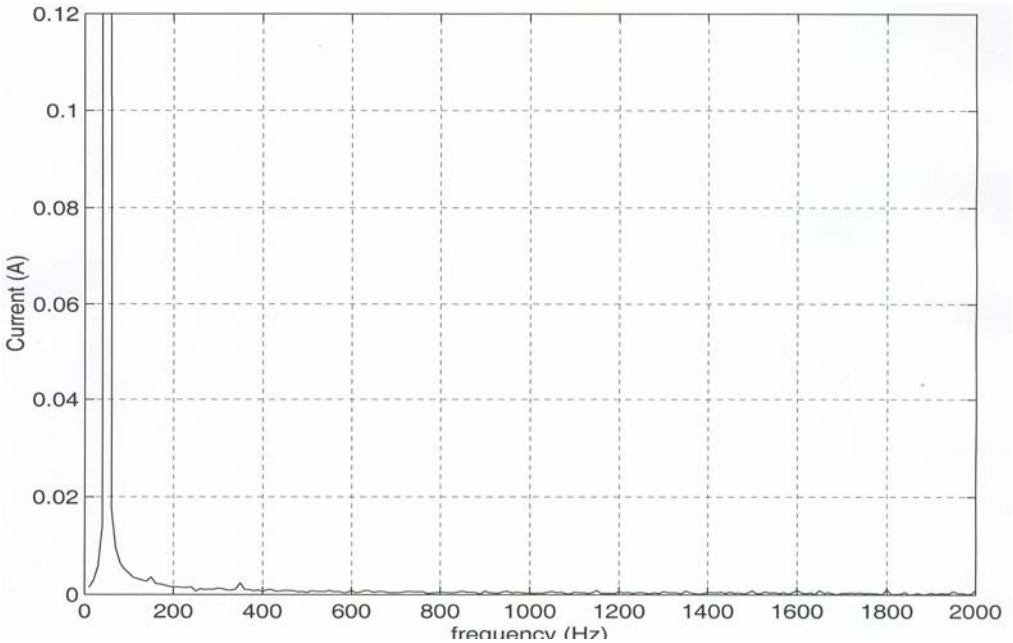
Simulation results of the low frequency current harmonics when the inverter current is much less than its rated value, in this case 0.5 A, are shown in Figures 3.19 (a) and (b). These results reveal that low frequency harmonics generated by the unipolar switched inverter increase significantly at low output power levels, while they remain negligible in the case of bipolar switched inverter. In the unipolar mode, the third harmonic (Figure 3.20) and the total harmonic distortion shown in Figure 3.21 also indicates that the power quality does significantly worsen when the inverter is supplying low power. Therefore it can be said that implementation delay is the main reason for the generation of low frequency harmonics, hence it cannot be ignored in design procedures.

The inverter in this project however, is being designed for a rated output of 4 A ($\hat{I}_s$ = 5.9 A) and would therefore satisfy the current Australian Standard [4] requirements even if implementation delay was as high as 8 μs (Figure 3.20). Individual levels for the second to the ninth harmonic have to be limited to 4% (or 0.237A) whereas total harmonic distortion needs to be limited to 5% at rated output (Table 3.3). Therefore, unipolar switched inverters are suitable for the proposed utility PV connected application.

The reasons for the presence of large amplitude of low frequency harmonics for non zero delay, when a unipolar switched inverter is used, is explained in the next section.



(a) Unipolar: Low frequency harmonics



(b) Bipolar: Absence of low frequency harmonics

Figure 3.19: Low frequency current spectra for inverter supplying 0.5 A (*td* = 8 μs)

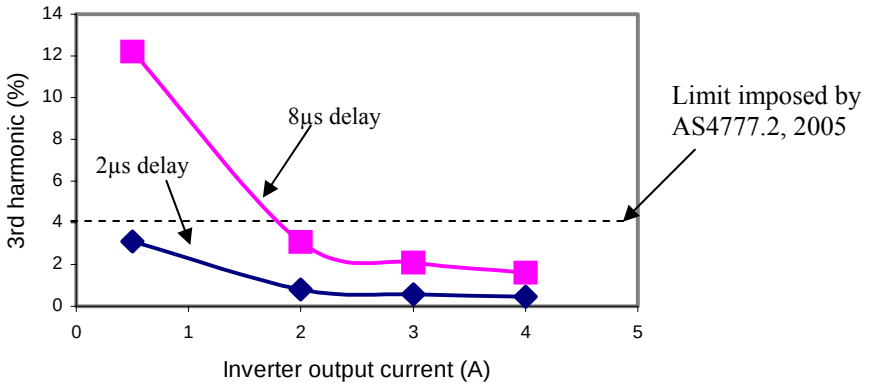


Figure 3.20: Unipolar: Effect of delay on the 3rd harmonic component

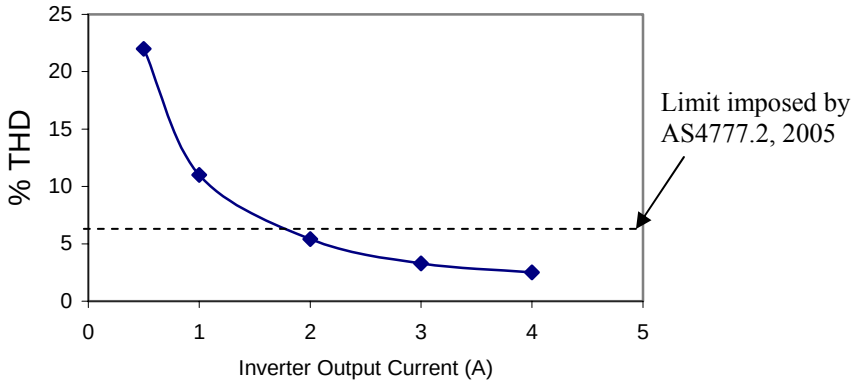


Figure 3.21 Unipolar: Total harmonic Distortion of output current (td = 8µs)

3.11. Origins of Low Frequency Harmonics

This section is an expanded version of a paper presented by Sharma and Ahfock at AUPEC 2004 [62].

With reference to Figures 3.5 and 3.22, for the inverter output current I_s to be a perfect sinusoidal waveform (free of low frequency harmonics), the difference between the area enclosed by each switching cycle above and below the reference current i_{sref} should be zero. However, for unipolar switched inverters, on the assumption that $\omega L \hat{I}_{sref} << V_c$, it can be shown using equations 3.20 and 3.22 that, $t_r > t_f$ when θ is less than $\theta \approx \sin^{-1} V_c / 2\hat{V}_s$, and $t_r < t_f$ when θ is greater than $\theta \approx \sin^{-1} V_c / 2\hat{V}_s$.

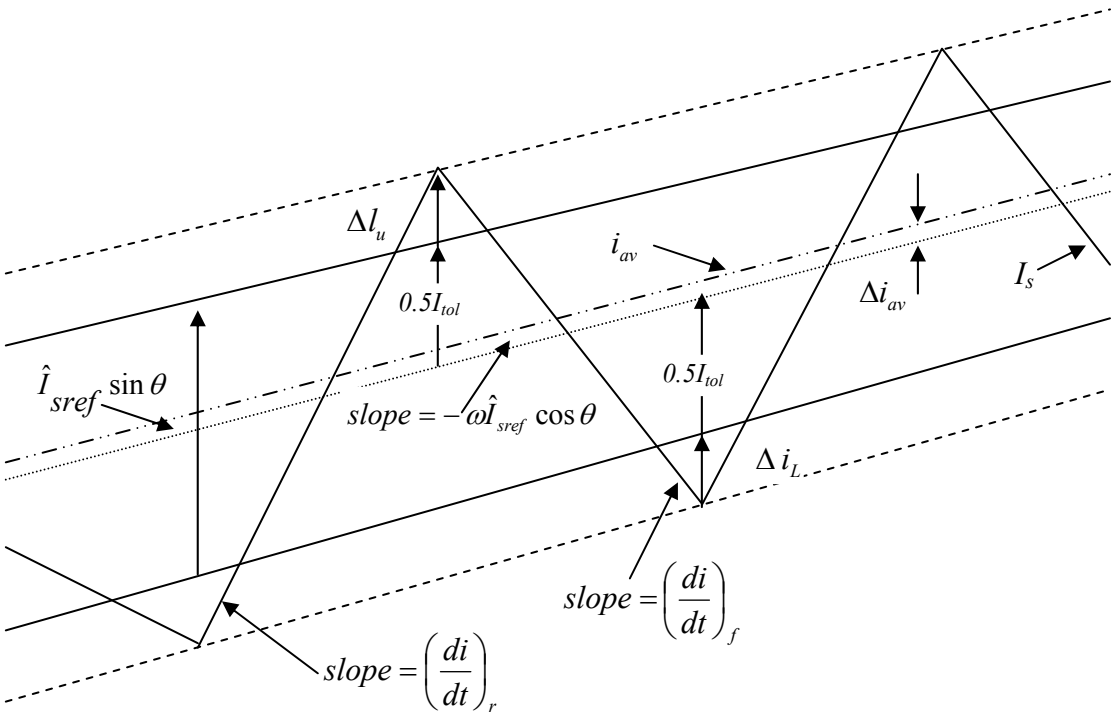


Figure 3.22 Average current Δi_{av}

Similarly, equations 3.29 and 3.31 can be used to show that for bipolar switched inverters, neglecting the term $\omega L \hat{I}_{sref}$, $t_r > t_f$ for all non-zero values of θ. To determine levels of current distortion in both cases, the average current along the current waveform needs to be determined.

Based on the assumptions made in section 3.3, expressions will be derived for the current i_{av} that represents the average of each switching cycle along the current waveform. Current i_{av}, although averaged, is a function of time and may be regarded as current i_s, with all the switching frequency harmonics, and the DC offset current being ignored. It will be shown in Chapter 5 that switching frequency harmonics are not a problem, because a simple ripple frequency filter can be used to remove them. Hence the presence of the low frequency current harmonics will be investigated with the switching frequency harmonics ignored. Similarly, DC offset removal is dealt with in Chapter 9, and is therefore ignored when determining the level of low frequency harmonics generated by unipolar switched inverters.

3.11.1. Presence of Low Frequency Harmonics using Unipolar Switching

With reference to Figure 3.22, the triangles above and below the average current, for each switching cycle, are similar triangles. Equating areas, the average current difference Δi_{av} for each switching cycle is given by:

$$\Delta i_{av} = \frac{1}{2}\left[\Delta i_u - \Delta i_L\right] \tag{3.36}$$

For unipolar, calculation of overshoot due to delay for the positive half cycle:

$$\Delta i_u = t_d\left[\left(\frac{di}{dt}\right)_r - \omega \hat{I}_{sref}\cos\theta\right] \tag{3.37}$$

$$\Delta i_L = t_d \left[-\left(\frac{di}{dt}\right)_f + \omega \hat{I}_{sref} \cos\theta \right] \tag{3.38}$$

The slopes of the straight line segments of the current waveform from equations 3.1 and 3.4:

$$\left(\frac{di}{dt}\right)_r = \frac{1}{L}\left[V_c - \hat{V}_s \sin\theta\right] \qquad \text{and} \qquad \left(\frac{di}{dt}\right)_f = -\frac{1}{L}\hat{V}_s \sin\theta$$

Therefore, $\Delta i_{av} = \frac{t_d V_c}{2L} - \frac{t_d \hat{V}_s}{L}\sin\theta - \omega t_d \hat{I}_{sref} \cos\theta$ (3.39)

The average current is:

$$i_{av} = i_{sref} + \Delta i_{av}$$

$$i_{av}(\theta) = \left(\hat{I}_{sref} - \frac{t_d \hat{V}_s}{L}\right)\sin\theta + \frac{t_d V_c}{2L} - \omega t_d \hat{I}_{sref} \cos\theta \tag{3.40}$$

Since the magnitude of the quadrature term is generally negligible by comparison, equation 3.40 can be written as:

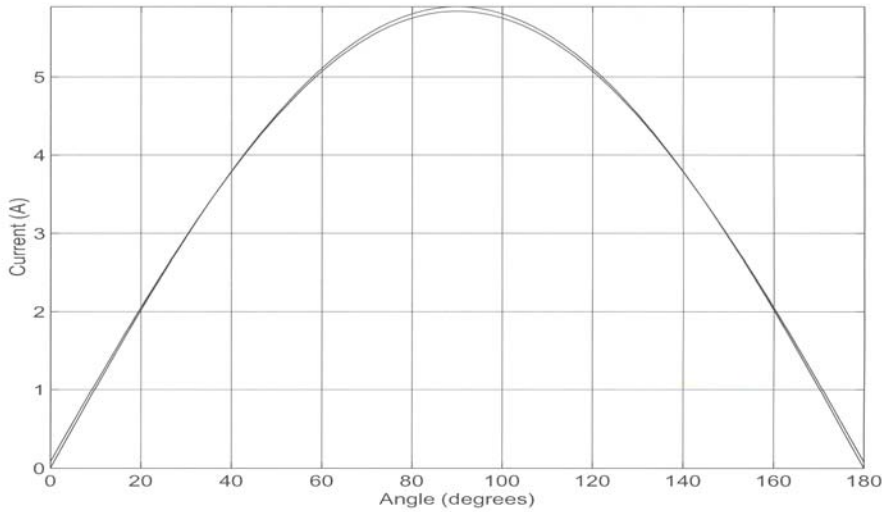
$$i_{av}(\theta) \approx \left(\hat{I}_{sref} - \frac{t_d \hat{V}_s}{L}\right)\sin\theta + \frac{t_d V_c}{2L} \tag{3.41}$$

The following can be deduced from equation 3.41:

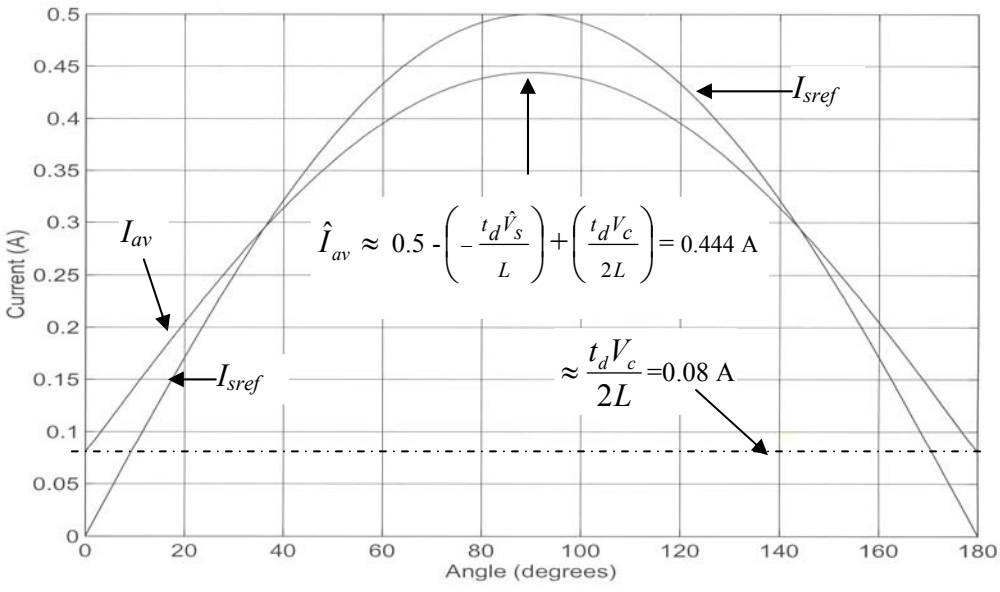
(a) If switching delay is set to zero, as expected, current i_{av} matches the reference current i_{ref} exactly.

(b) A non-zero switching delay results in i_{av} being higher than i_{ref} for half of the time and lower for the other half (Figure 3.23). The value of i_{av} is less than i_{ref}

for half the cycle because of the term $\left(-\frac{t_d\hat{V}_s}{L}\right)$ in equation 3.41. However, this does not contribute to the presence of low frequency harmonics.



(a). Inverter supplying a peak current of 5.9 A



(b). Inverter supplying peak current of 0.5 A

Figure 3.23: Unipolar switched inverter: output current with 4µs delay

(c) Distortion of the current i_{av} signifying the presence of low frequency harmonics can be better shown at lower inverter output current (Figure 3.23 (b)). The fixed term in equation 3.41, changes sign each half cycle and forms approximately a square wave with amplitude of $\approx\left(\frac{t_d V_c}{2L}\right)$, becoming more significant as I_s decreases. During the negative half cycle the term is negative. The square wave contributes to all the odd harmonics whose peak amplitudes are given by:

$$I_{sn} \approx \left(\frac{t_d V_c}{2L}\right)\frac{4}{n\pi} \qquad \text{where n is an odd number.} \qquad (3.42)$$

Numerical values of low frequency harmonics generated by the square wave component in equation 3.41 are shown in Table 3.4. The current loop SIMULINK simulation results using the same CCL component values are shown in Figure 3.24. The numerical values of the low frequency harmonics shown in table 3.4 are very close to the FFT values of the inverter output current using the SIMULINK model of the CCL. Therefore, the numerical values of V_c, t_d and L (equation 3.24) can be used by inverter designers to estimate the magnitude of the lower order harmonics.

However, the suitability of using equation 3.42 largely depends on the value of I_{sref} and L. For example, if the inverter output is increased from 1 kW to 2 kW, the difference between the results obtained using the two methods, increases from negligible to about 15%. This is expected, because an increase in the inverter output also produces an increase in F_{min} (low frequency harmonics are influenced by F_{min}; equation 3.24) from 5.146 kHz to 10.290 kHz. On the other if L is reduced from 10 mH to 5 mH, the difference in the results obtained using the two methods is negligible even at 2 kW. Therefore, when using the numerical approach, the magnitude of the term $-\omega t_d \hat{I}_{sref}\cos\theta$ with respect to the square wave term in equation 3.40, should be examined.

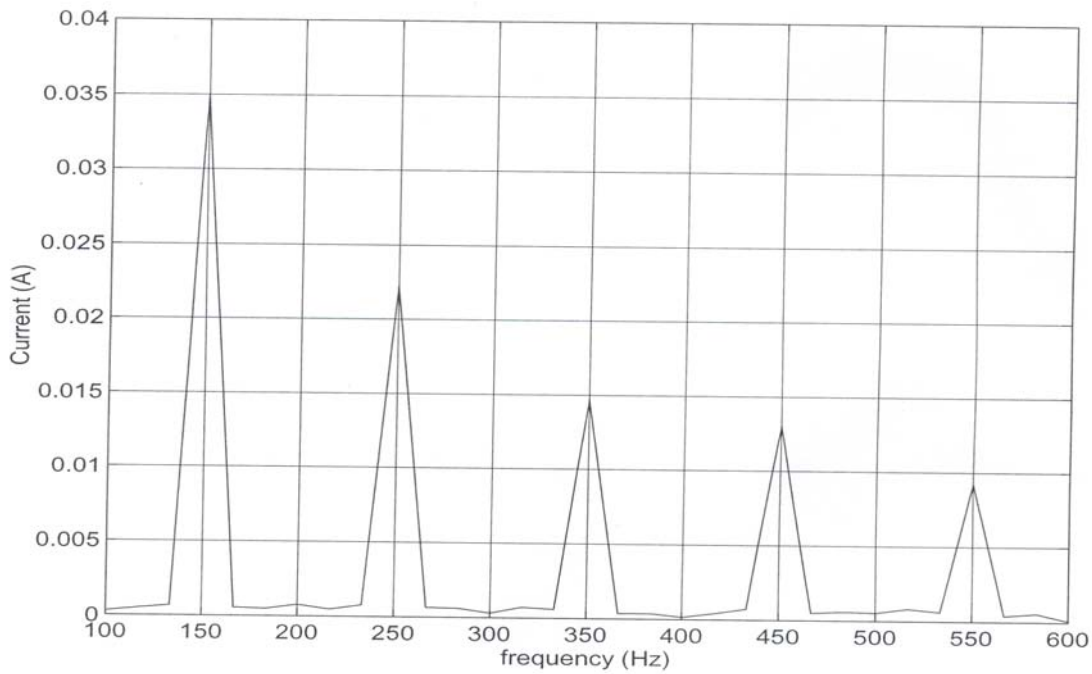


Figure 3.24 FFT of simulated Inverter output current (I_s = 0.5 A and t_d = 4μs)

Low Frequency Harmonics	Calculated (Square wave contribution)	Simulation results (from Figure 3.17)
Third (I_{s_3})	0.034 A	0.035 A
Fifth (I_{s_5})	0.0204 A	0.022 A
Seventh (I_{s_7})	0.0145 A	0.015 A
Ninth (I_{s_9})	0.011 A	0.0125 A
Eleventh ($I_{s_{11}}$)	0.009	0.009 A

Table 3.4: Numerical values of Low frequency harmonics (I_s = 0.5 A and t_d = 4μs)

3.11.2. Absence of Low Frequency Harmonics using Bipolar Switching

For bipolar mode, the average current i_{av} can be obtained using the same process as that used for the unipolar mode. The only difference is:

$$\left(\frac{di}{dt}\right)_f = -\frac{1}{L}\left(V_c - \hat{V}_s \sin\theta\right) \tag{3.43}$$

Hence, $\Delta i_{av} = -\frac{t_d \hat{V}_s}{L}\sin\theta - \omega t_d \hat{I}_{sref}\cos\theta$ (3.44)

and $i_{av}(\theta) = \left(\hat{I}_{sref} - \frac{t_d \hat{V}_s}{L}\right)\sin\theta - \omega t_d \hat{I}_{sref}\cos\theta$ (3.45)

Again, since the term $\omega t_d \hat{I}_{sref}\cos\theta$ is very small, equation 3.45 can be approximated to:

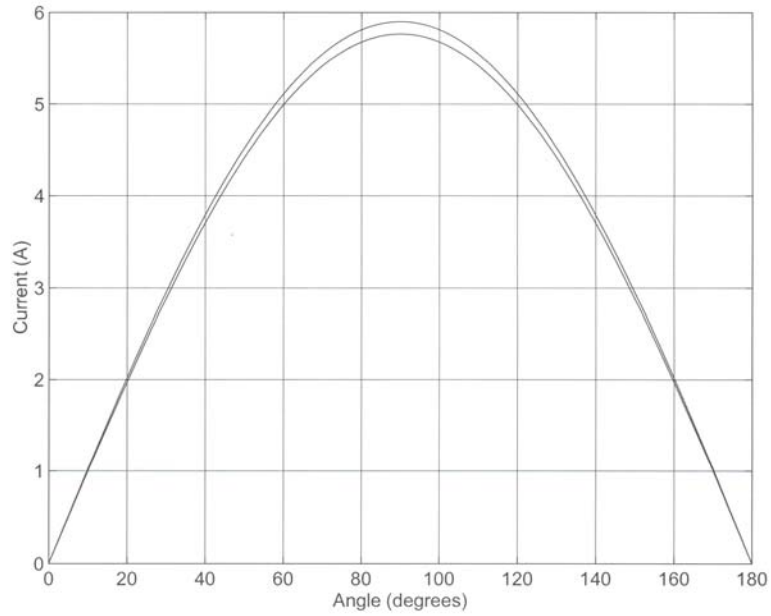
$$i_{av}(\theta) \approx \left(\hat{I}_{sref} - \frac{t_d \hat{V}_s}{L}\right)\sin\theta \tag{3.46}$$

The following can be deduced from equation 3.46:

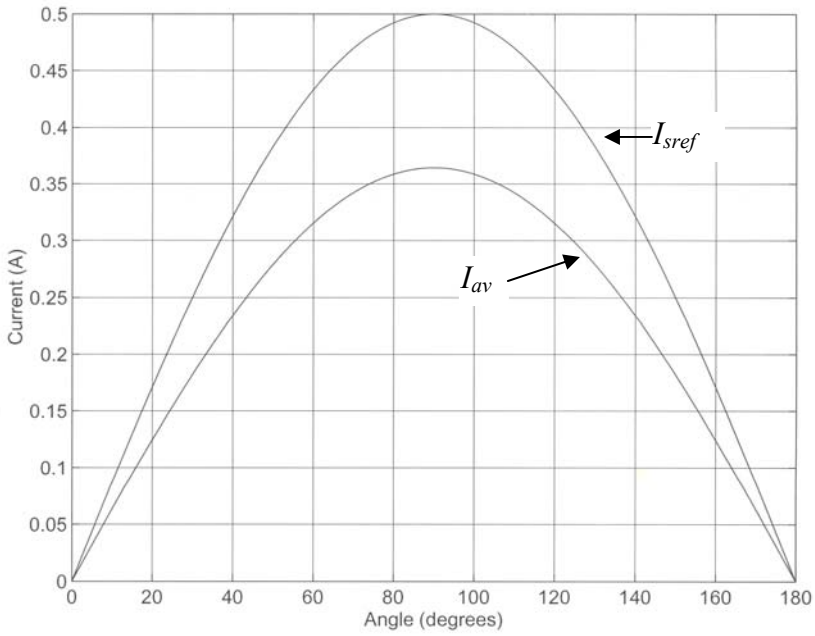
(a) As in the unipolar case, if the switching delay is set to zero current i_{av} matches the reference current exactly.

(b) Average current i_{av} is always lower in magnitude than i_{sref} by a factor of $\left(-\frac{t_d \hat{V}_s}{L}\right)$. This signifies that although i_{av} is lower than i_{sref}, there are no low frequency harmonics because i_{av} is a sine wave.

(c) The relative difference between current i_{av} and current i_s is higher at lower inverter output current (Figure 3.25) because the term $\left(-\frac{t_d \hat{V}_s}{L}\right)$ becomes more significant. This is illustrated in Figure 3.25.



(a) Inverter supplying 4.0 A



(b) Inverter supplying 0.5 A

Figure 3.25: Bipolar switched inverter: Output current waveforms for t_d = 4μs

3.12. Conclusions

Work carried out in this chapter has resulted in the following conclusions:-

- New theoretical models that included implementation delays have been successfully developed to determine switching frequencies along a current cycle for both unipolar and bipolar switched inverters.

- It has been shown that the generation of low frequency harmonics in unipolar switched inverters using hysteretic current control is due to implementation delays.

- A new switching model to determine the average value of the inverter current has been developed to explain why these low frequency harmonics are generated in unipolar switched inverters but are absent in bipolar switched inverters.

- Despite being inferior to bipolar switched inverters with respect to generation of low frequency harmonic currents, it has been shown that unipolar inverters can be designed to meet the requirements of Australian Standard AS4777.2, 2005. Suggestions to reduce low frequency current harmonic generated by unipolar switched inverters will be discussed in Appendix C.

Finally, theoretical results presented in this chapter have established that current harmonics injected into the grid supply using the unipolar mode can be maintained at an acceptable level, and hence a unipolar switched inverter will be used in this project. Advantage will be taken of lower power losses, simpler current control circuit requirements and lower EMI generation features of unipolar switching to achieve the aims of this project. Bipolar switched inverters will not be discussed any further.

The design and construction of the circuits for the current loop based on the findings in this chapter, together with the experimental results with respect to its performance, will be presented in the next chapter.

CHAPTER 4

CURRENT LOOP: DESIGN AND TESTING

4.1. Introduction

The purposes of this chapter are; firstly to describe the practical implementation of the current control loop for the unipolar switched inverter system designed in Chapter 3; secondly, to present experimental results of the main sources of implementation delays and finally, to present techniques employed to minimise these delays during the circuit design process. The circuits used for the current control loop (CCL) are discussed in detail.

The most cost effective method of preventing unwanted high frequency switching noise from corrupting the inverter output current is to suppress it at its source. It is shown in this chapter that a unipolar switched inverter can be made less susceptible to its own switching noise, without compromising the efficiency, cost and power quality of the inverter system. Results are presented to show that this advantage of unipolar switching can be achieved by choosing the appropriate switching combinations of the inverter switches. Hence, a low noise inverter output current has been realised without the need for additional RFI filters in the current feedback loop.

To avoid malfunctions of the inverter-bridge, care has been taken to ensure that the operation of the inverter is not adversely influenced by the unwanted communication/control signals used by the local power supply authorities, or by other non-linear loads connected to the point of common coupling. The methods used to minimise the effect of such communication signals are also presented in this chapter.

4.2. Choice of Current Loop Components

The relationship between the inverter current loop variables (V_s, V_c, I_{Tol}, L, t_d) and lower order harmonics was discussed in Chapter 3. In equation 3.40 (Chapter 3), the term $\left(\frac{t_d V_c}{2L}\right)$ was approximately equal to the amplitude of a square wave component of the inverter output current, responsible for the lower order harmonics. The aim of this subsection is to determine the values of V_c, L and t_d, such that the level of low frequency harmonics generated by the current loop is as small as possible.

The value of $\hat{V}_s$ is fixed by the supply authority and the upper limit ($\hat{V}_s$+6%) is 360 V. With reference to equation 3.42, to minimise lower order harmonics, V_c should not be very much greater than 360 V. The effect of changes in V_c and L on the generation of third harmonics I_{s3} is shown in Figure 4.1 This result illustrates that the actual increase in I_{s3} due to a 30 V increase in V_c is very small. However, in section 3.6 (Chapter 3), for the tolerance band to be able to control the switching frequency, the circuit delays t_d must obey the inequality $t_d V_c < I_{tol} L$. Increasing V_c therefore magnifies the effect of the circuit delays t_d. Based on these results, the value of V_c chosen was 400 V. This would have negligible effect on the low frequency harmonics and on the performance of the current tolerance band I_{Tol}.

With reference to Figures 4.1 and 4.2, it is clear that a reasonable compromise between minimisation of switching harmonics and increasing inductor power losses would be achieved by selecting an inductor value of 10 mH. While the use of higher than 10 mH reduced low frequency harmonics, it will be at the expense of higher power losses. On the other hand, use of 5 mH for L will result in lower losses but the low frequency harmonics will be much higher. Therefore, the total inductance of the outer loop, chosen for the practical test was 10 mH.

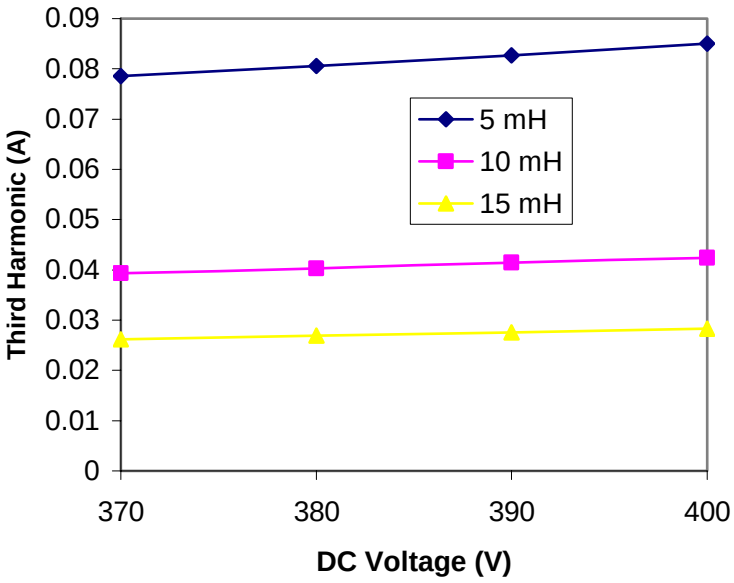


Figure 4.1: Effect of changes in V_c and L on third harmonic (t_d = 5 µs)

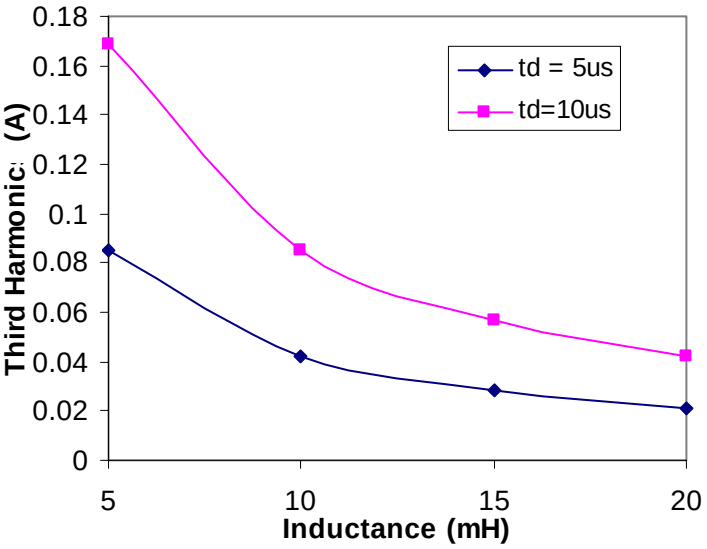


Figure 4.2: Effect of changes in t_d and L on third harmonic (V_c = 400 V)

4.3. Minimising Switching Noise Interference

Figure 4.3 shows the current loop of the inverter-bridge responsible for converting the DC output current from the solar panels to sinusoidal AC current. Insulated gate bipolar transistors (IGBTs) are used to perform the switching functions. The advantage of the IGBT is that its conduction losses are lower than that of the power MOSFET.

Each diagonal pair of switches in the inverter-bridge shown in Figure 4.3 executes two functions, as determined by the current controller. Firstly, a pair of switches operates to change the polarity of the DC voltage across the inductor *L* at the end of each half cycle, in this case every 10 mS (unipolar mode). Secondly, one of the pair must operate at switching frequencies to force the current to stay within a small tolerance band around a reference current i_{sref}. A Hall Effect current sensor was used to provide a feedback voltage proportional to the current I_s. It was chosen because of its low cost and its frequency range of DC to 25 kHz which was considered desirable.

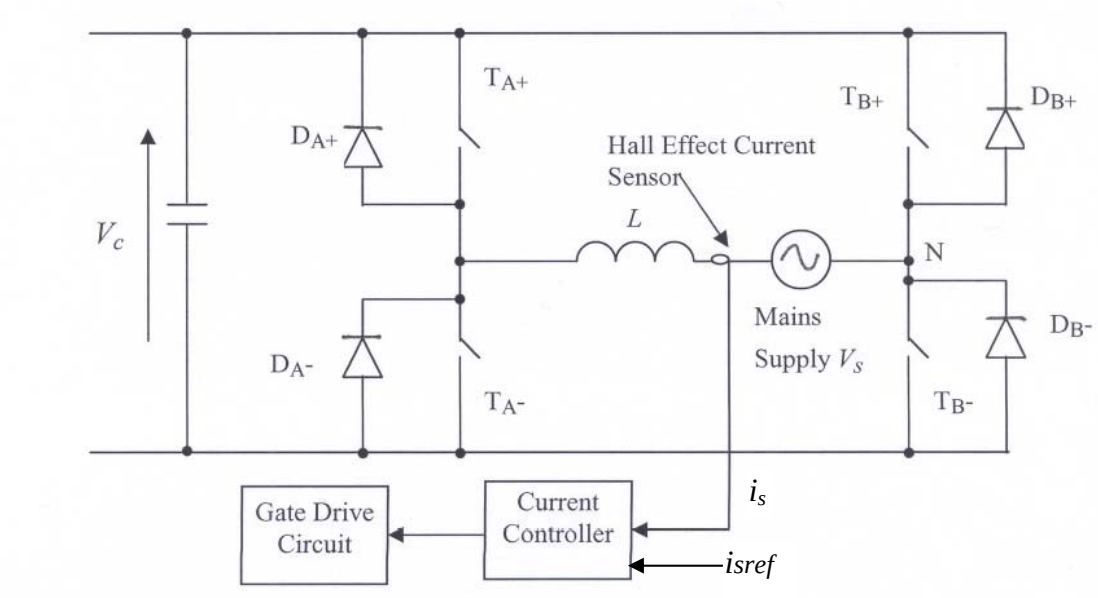


Figure: 4.3: Inverter current loop without switching frequency filter

The problems of switching signals being corrupted by interference, using hysteretic current control, were discussed in chapter 2. Possible solutions to overcome this problem such as, using constant frequency modulation, variable hysteresis band

methods and superimposing a common offset signal were presented also in Chapter 2 [33, 36-43]. In this subsection it is shown that the switching action tends to corrupt the reference current causing irregular switching. A simple solution that requires no addition circuitry or additional cost is proposed to overcome the interference problems in hysteretic current control unipolar switched inverters.

As shown in Table 4.1, theoretically, there are four equivalent options for controlling the inverter bridge. To implement option 1, at the start of the positive half cycle of the current $i_{s,}$ switches T_{A+} and T_B- are turned on. Only T_{A+} remains on, as long as i_s stays positive. During this positive half cycle, switch T_B- changes state each time i_s goes outside the tolerance band. When the magnitude of i_s has to be decreased, device D_{B+} operates, and T_{A+} remains on.

Similarly, at the start of the negative half cycle of the current i_s, both T_{B+} and T_A- are turned on, but only T_{B+} changes state every time i_s goes outside the tolerance band. During this half cycle, T_A- and D_B- operate to decrease $|i_S|$. The switch operations for the remaining options can be explained in a similar manner.

Option	Conducting Frequency	Switch Combinations
1	100 Hz	T_{A+} or T_A-
	Switching Frequency	T_{B+} or T_B-
2	100 Hz	T_{B+} or T_B-
	Switching Frequency	T_{A+} or T_A-
3	100 Hz	T_{A+} or T_{B+}
	Switching Frequency	T_A- or T_B-
4	100 Hz	T_A- or T_B-
	Switching Frequency	T_{A+} or T_{B+}

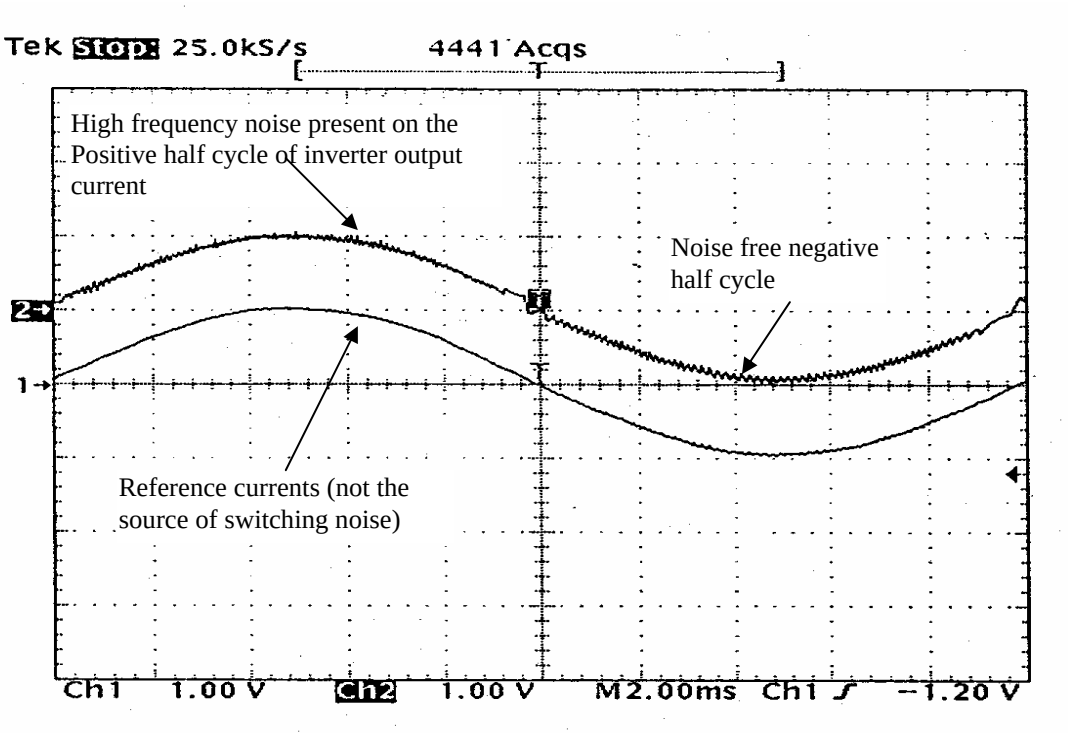
Table: 4.1 Equivalent unipolar switching options

Only one of these four combinations together with the location of the Hall Effect current sensor as shown in Figure 4.3 will result in significant reduction in the high

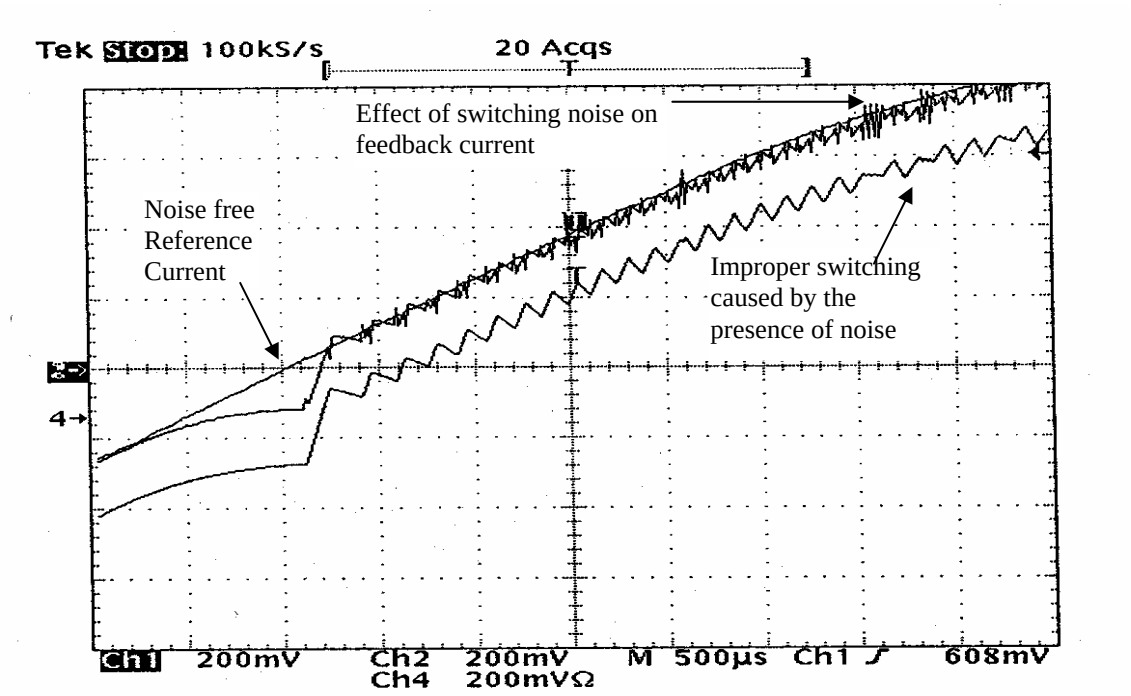
frequency electrical noise present in the feedback current, and in the inverter output current. Choice of any incorrect option will corrupt the current feedback signal, and may cause inverter failure due to improper switching. Experimental results to demonstrate this problem are shown in Figures 4.4 (a) and (b). The traces shown in Figure 4.4 have been deliberately offset to show the presence of noise and its effect on the feedback current and the inverter output current.

Of all the four possible options, if option 2 is chosen and the current sensor is located as shown in Figure 4.3, the conducted high frequency switching noise in the feedback current is attenuated. This is confirmed by the experimental results shown in Figure 4.4(c). In this arrangement the ferrite core inductor *L* shields the current sensor from the high frequency switching noise when T_{A+} and T_{A}- are operating. The inductor and the stray capacitances between the inductor winding and earthed inductor enclosure act as a low pass filter to shunt the conducted RF noise. The operation of switches T_{B+} and T_{B}- does not affect the feedback current because these switches only operate when the inverter output voltage and current are zero.

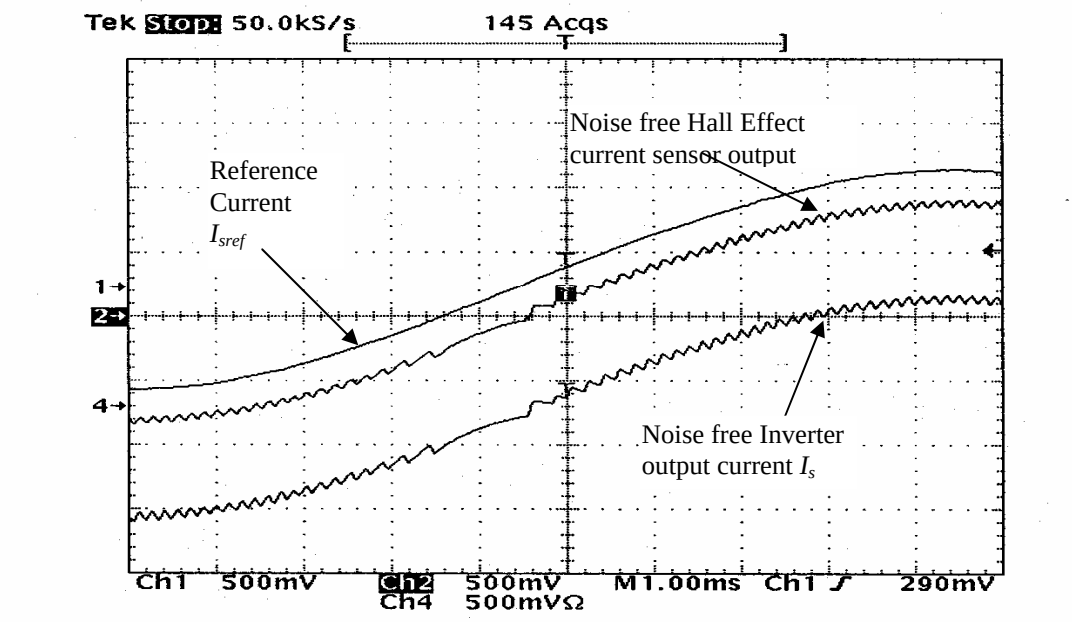
It is this feature of the unipolar mode that gives designers the opportunity to minimise the effect of electrical noise caused by the switching action, at no extra cost. The flexibility to choose different switching combinations is not available in the bipolar mode, as both switches of each diagonal pair must operate simultaneously. One pair is turned on when the current is to be increased and the other pair operates when the current must be decreased.



(a): Measurements showing current corrupted by unwanted switching noise using option 1 (Table 4.1).



(b): Measurements showing improper current switching due to unwanted switching noise using option 1(Table 4.1)



(c): Noise free inverter output current using option 2 (Table 4.1)

Figure 4.4: Measurements showing the effect of switching noise on the operation of the CCL

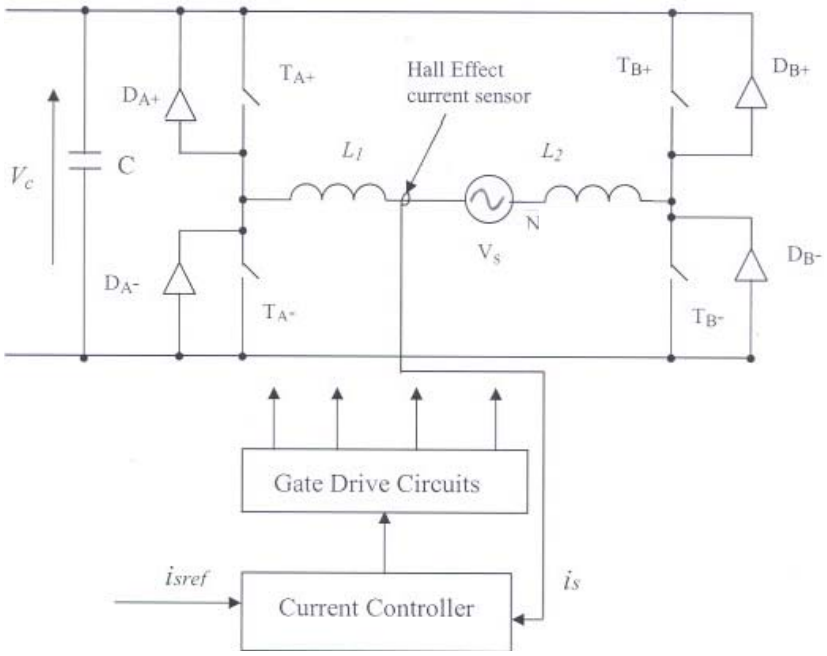


Figure 4.5: Inverter current loop with split AC inductor

While experimental results using a single inductor L as shown in Figure 4.3 produced no improper switching at the zero crossing of the inverter current, the split inductor arrangement shown in Figure 4.5 is preferred. The two inductors are wound on separate ferrite cores to minimise mutual coupling. Since a transformerless inverter system is being proposed in this project, the split inductor arrangement provided the following additional benefits: -

a) Dead time has been allowed between T_{B+} turning off and T_B- turning on as a precaution to prevent any unwanted switching at the zero crossing. Unwanted switching may occur due to the effect of stray capacitance (C_{stray}) across T_{B+}, T_B-, D_B-, D_{B+} and the earth loop via the neutral conductor (Figure 4.3). Since V_c is large, C_{stray} may give rise to stray currents ($i_{stray} = C_{stray} \frac{dV_c}{dt}$) even when I_s is zero. The proposed split inductor arrangement can be used to minimise the effect of i_{stray} on the performance of other equipment connected at the PCC.

b) The sum of the inductance of the split inductors is equal to the original single inductor ($L = L_1 + L_2$). Therefore, the inductors can be designed such that the power losses are not increased.

c) It will be shown in chapter 5 that the ratio of L_1 and L_2 can be chosen to optimise ripple current filtering.

4.4. Current Loop Circuit Design

Following the successful design of the maximum power point tracker (presented in Appendix A) using a microprocessor, the initial current controller was designed using the same digital technology. However, it was found that the maximum switching frequency was not acceptable for the proposed application. The analog to digital conversion process of the voltages and currents, combined with the comparison process (I_s and I_{sref}) limited the minimum switching frequency to less than 2 kHz. However, Boys and Green [24] recommended that inverter switching frequencies should be greater than 2 kHz. Hence, analog circuits were chosen to test the design principles and to confirm the effects of circuit delays on the performance of a unipolar inverter system. The analog circuits chosen for testing purposes were more cost effective, less prone to failures during testing, and allowed greater flexibility to investigate each stage of the inverter separately.

The simplified circuit diagram of the hysteretic current controller is shown in Figure 4.6. The corresponding test circuit and the final printed circuit of the current controller are given in Figures 4.7 (a) and 4.7 (b).

As stated earlier, the function of the current controller is to force the inverter output to stay within a small tolerance band around the sinusoidal reference i_{sref} provided by the voltage control loop. Both i_s from the Hall Effect current sensor and i_{sref} are buffered using voltage followers (TC2 and TC3). Since the reference i_s is phase-

shifted by 180°, when added to i_{sref}, the magnitude of the resultant error (i_e) is very small. Hence

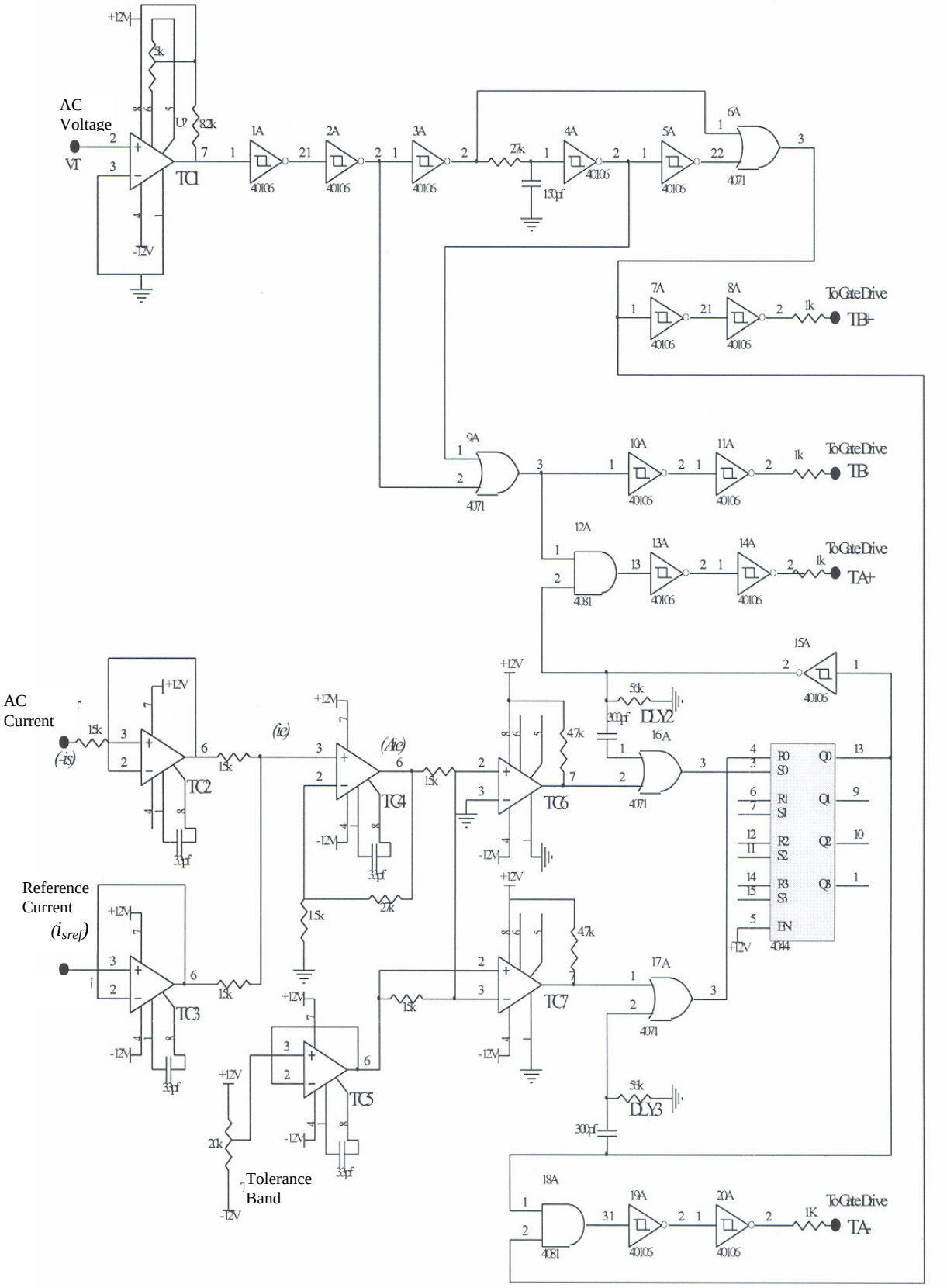


Figure 4.6: Schematic diagram of current controller

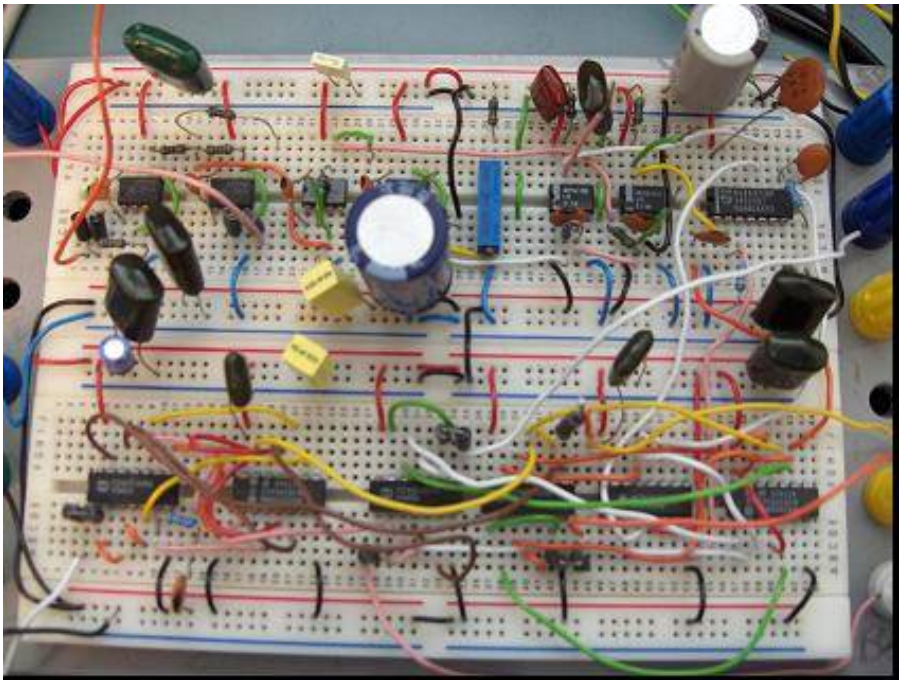


Figure 4.7 (a): Current controller test circuit

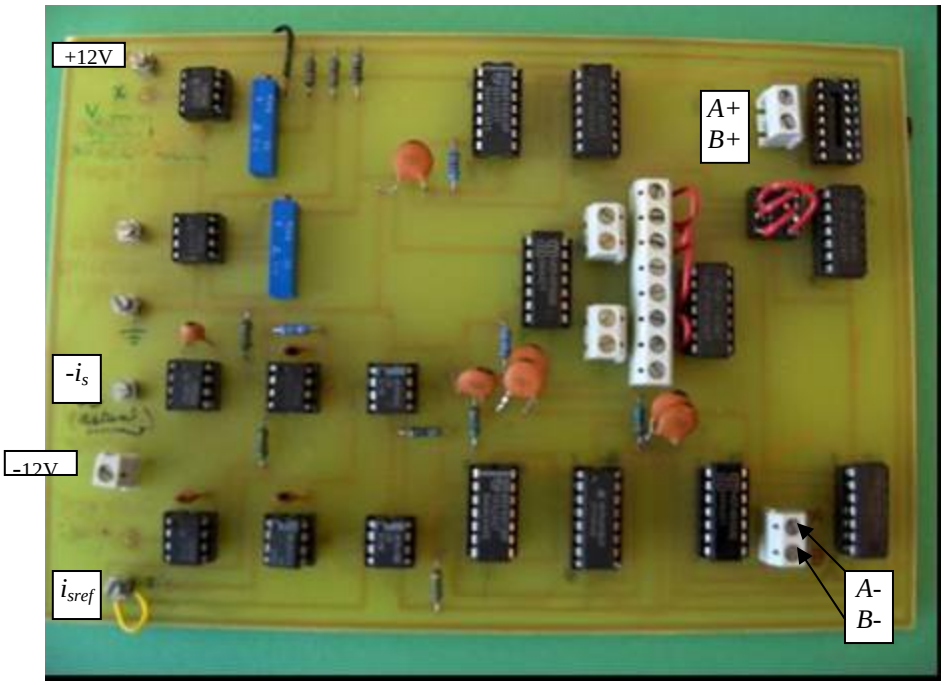


Figure 4.7 (b): Current controller printed circuit board

i_e is amplified by non-inverting amplifier TC4, giving an output current Ai_e, where A is the gain of the amplifier TC4.

The tolerance band magnitude i_{tol} is buffered (TC5) and added to Ai_e at inputs 2 and 3 of comparators TC6 and TC7 giving an upper and lower limit error current equal to (Ai_e+ i_{tol})/2. From this it can be deduced that when: -

$i_e > i_{tol}$, the output of TC6 is high

$i_e < i_{tol}$, the output of TC6 is low

$i_e < i_{tol}$, the output of TC7 is high

$i_e > i_{tol}$, the output of TC7 is low

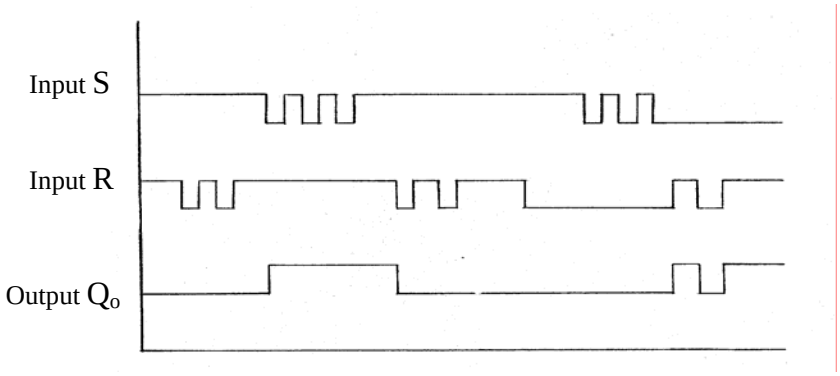


Figure 4.8 Timing waveform of R/S Latch

Using this method to provide a tolerance band ensured that the symmetry of the inverter output current waveform was maintained. As explained in Chapter 3, the magnitude of the tolerance band is chosen to limit the maximum switching frequency and to keep the distortion i_s at an acceptable level.

The outputs from the voltage comparators TC6 and TC7 provide the low active set and reset signals to the tri-state NAND R/S latch. The timing waveforms of the R/S latch showing the SET (S) and the RESET (R) inputs and the output Q_o are shown in

Figure 4.8. With logic 1 applied to the ENABLE input, the timing diagram can be explained as follows: -

- When the input S is low then the output Q_o follows the switching signal applied to input R
- When S is high then Q_o follows R only when R goes low (Q_o is not affected when R goes high)
- When R is low then Q_o is not affected by the input signal to S
- When R is high then Q_o goes high only when S goes low (Q_o is not affected when S goes low)

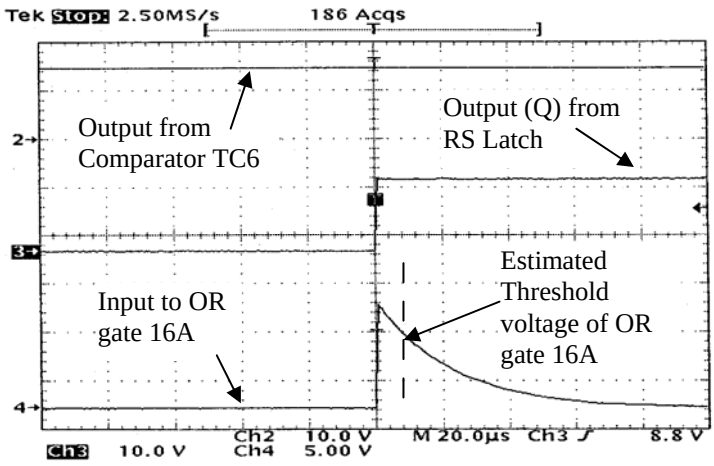


Figure 4.9: Measurement of minimum IGBT on-time

The proper operation of the R/S latch can be affected by unwanted noise present in the control signal applied to the R and S inputs. The use of two OR gates (16A & 17A) between comparators (TC6 & TC7) and the R/S latch input was to reduce the possibility of unwanted switching. Any noise on the switching signal immediately after the switching action may cause the comparator outputs to change state and this could lead to short-circuiting of the DC voltage supply. Unwanted switching was avoided by keeping the IGBTs switches T_{A+} or T_A- in leg A of the bridge (option 2

Table 4.1) on for a minimum period determined by the time-constant of DLY2 and DLY3. Any noise generated by the switching event will not interfere with the proper operation of the bridge with the inclusion of this delay. With reference to the R/S latch, once Q_o goes high, the output from the comparators will not be able to reset R until after the minimum on time as shown in Figure 4.9. Hence, when either switch T_{A+} or switch T_A- is turned on, it will remain on for the minimum time irrespective of the output from comparators TC6 or TC7 changing state. This minimum on-time is a precautionary measure and is governed by value of the implementation delay t_d.

Since the IGBTs from the two legs of the unipolar switched bridge using option 2 (Table 4.1) are not switched simultaneously, a zero crossing detector controls leg B separately. The input to the comparator TC1 is from the secondary of the voltage transformer VT. This voltage can be influenced by other power electronic equipment connected to the same power line or by the low frequency control/communication signals used by the local power supply authorities. Figure 4.10 shows unwanted change over of switches T_{B+} and T_B- caused by such signals at the zero crossing. This can lead to the distortion of the inverter output current (Figure 4.11) and in the worst case scenario may lead to the short-circuiting of the input DC voltage supply. By using a simple filter at the output of VT, unwanted switching is eliminated as shown in Figure 4.12.

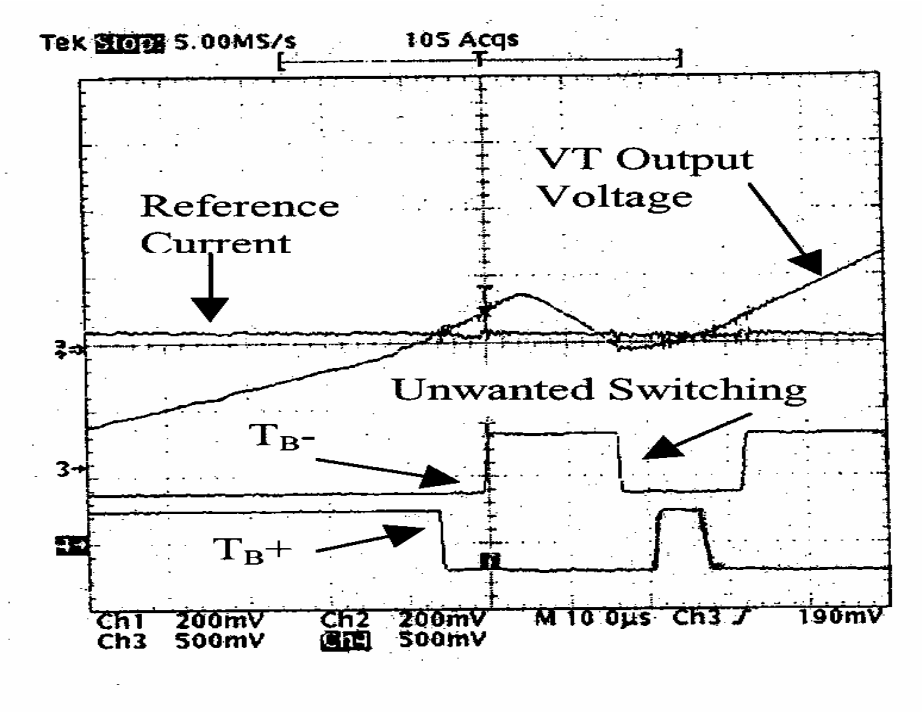


Figure 4.10: Influence of signal generated by other equipment at zero crossing

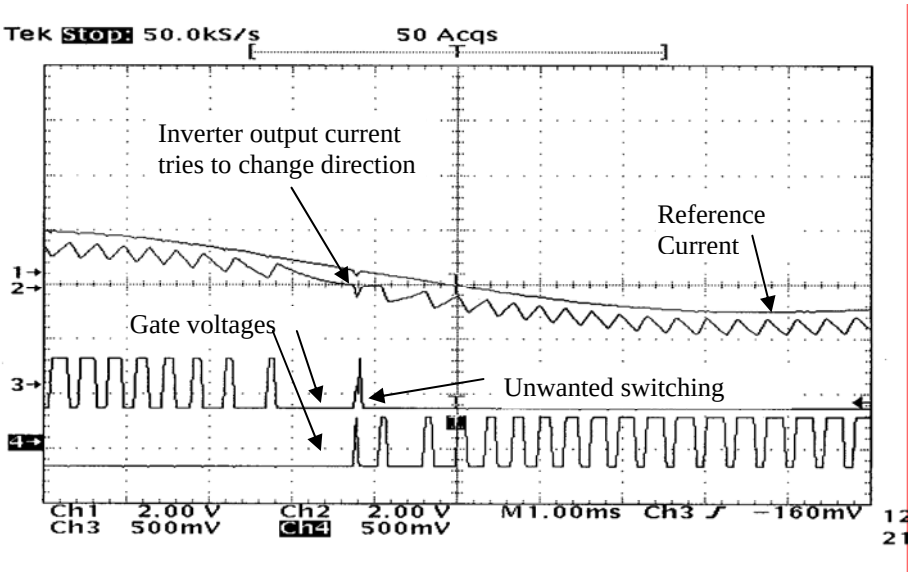


Figure 4.11: Unwanted switching due to signals from other equipment

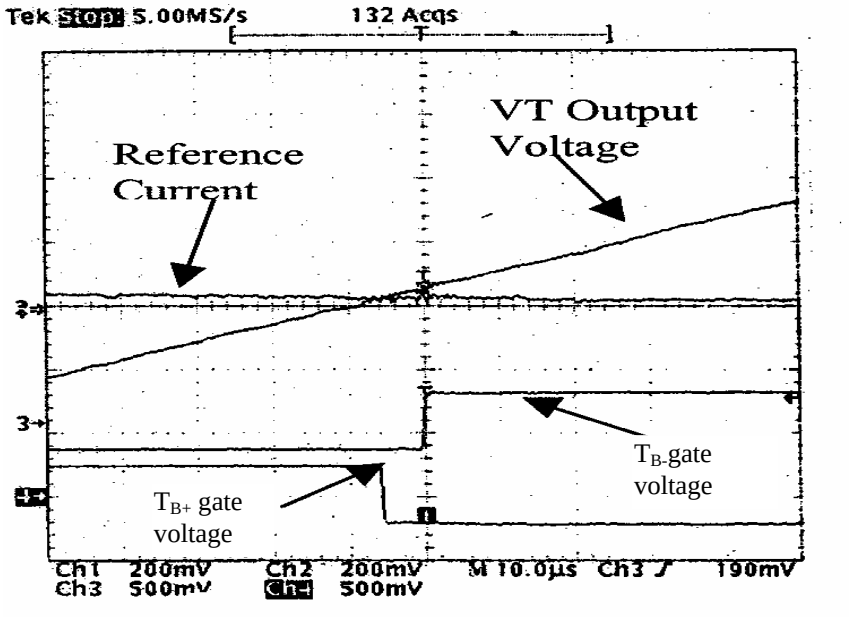


Figure 4.12: Removal of unwanted switching

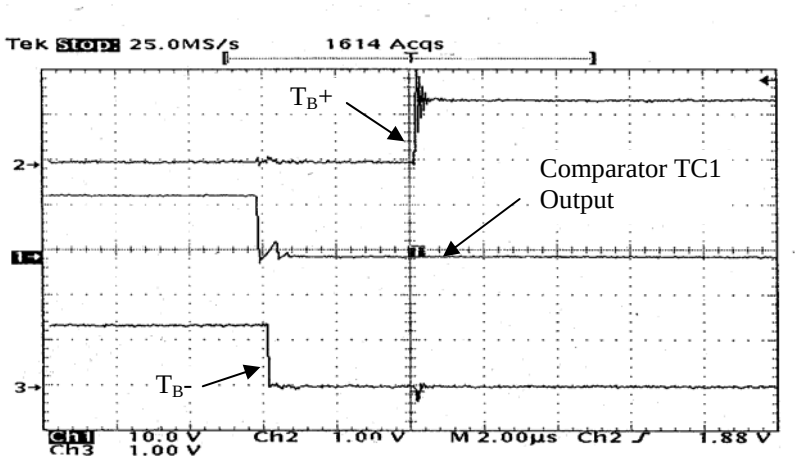


Figure 4.13: Inclusion of Blanking Time

The output from TC1 goes high when the supply voltage v_s goes positive and it remains high until v_s goes negative. During this period T_B- follows the output of TC1 and also remains high, while T_{B+} remains off. Using Schmitt Trigger A3, the output from TC1 is inverted so that when its output goes low, T_{B+} turns on and remains on during the negative half cycle. The delay DLY1 is necessary to ensure that all the bridge switches are off to prevent the short-circuiting of V_c during the reversal of V_s. The actual value of this blanking time is determined by the time constant of DLY1 and magnitude of the implementation delay t_d. Experimental results illustrating the effect of blanking time are shown in Figure 4.13 where T_{B+} turns on 4 µs after T_B- has turned off.

The purpose of the Schmitt Trigger between the output of the AND gates and the input to the gate drive was to reduce noise in the switching signals that may have been introduced by the comparators.

Finally, to test the inverter system, the total inductance of the current loop was kept the same as the value (L_1 + L_2 = 10 mH) used to obtain the theoretical results in Chapter 3. To minimise unwanted switching, the values chosen for L_1 and L_2 were 8 mH and 2 mH respectively. The capacitance of the input filter capacitor C was chosen to be 2000 µF. The use of the same CCL values will allow comparisons between the theoretical results and the experimental results to be made.

4.5. Experimental Results

To validate the theoretical results obtained in Chapter 3, the first step was to measure the total current loop circuit delay t_d. These measured values of t_d were then substituted in equations 3.23, 3.24 and 3.25 (Chapter 3) to enable realistic comparisons of the simulation and experimental values for F_{min}, F_{med} and F_{max} to be carried out.

As shown in Figure 4.6, there are separate circuits controlling each pair of the four inverter IGBTs, T_{A+}, T_{A-}, T_{B+} and T_{B-} and therefore the propagation delays of each of these branches had to be measured separately. The total delay of the circuit operating switches B^+ and B^- (leg B of the bridge shown in Figure 4.5) at 100 Hz was about, 18 μs. This result is shown in Figure 4.14, where the inverter IGBT switches change over 18 μs after the reference current passes through the zero crossing.

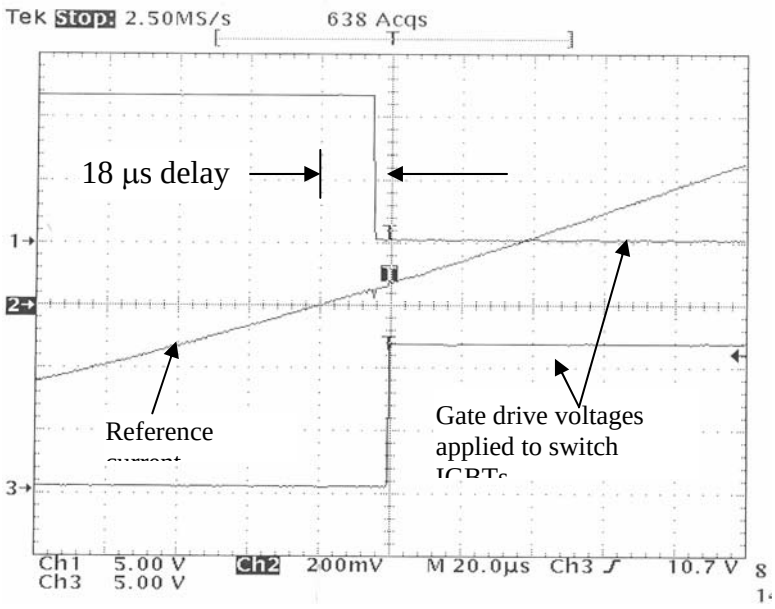


Figure 4.14: Total measured delay for leg B of inverter-bridge

Similar measurements of the input signal to and the output signal from the gate drive circuit revealed that the drive circuit was responsible for only 2 μs of this 18 μs delay (Figure 4.15). Methods to reduce the 16 μs delay introduced by the zero detecting circuit will be discussed later.

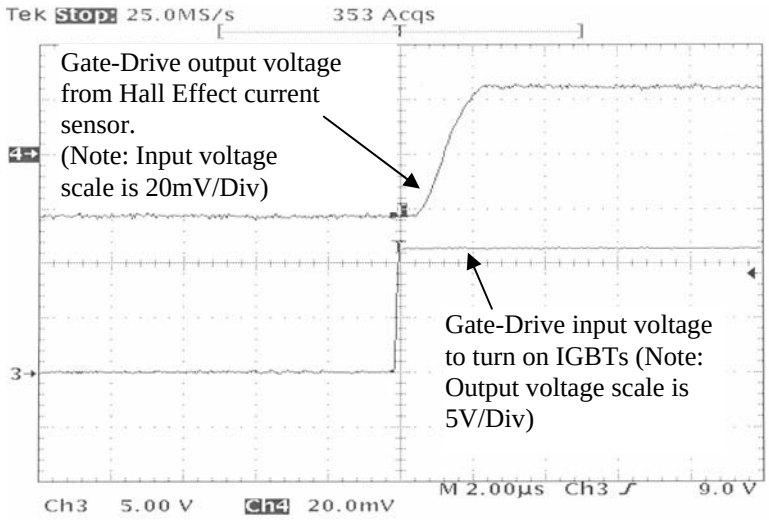


Figure 4.15: Measurement of gate drive delay

Similarly, measurement of the delay in the operation of switches T_{A+} and T_{A-} (leg A of the bridge shown in Figure 4.5) at the switching frequencies, revealed that the Hall Effect current sensor contributed about 16 μs towards the total delay as illustrated by Figure 4.16. The current sensor delay comprises propagation delay, phase shift and attenuation of the feedback signal above the 3dB cut-off frequency of 25 KHz.

It should however be pointed out that the measured values of propagation delays for the A and B legs of the inverter bridge included small delays introduced by the measuring instruments. Since the minimum bandwidth of these instruments (current probe) was 40 MHz, the measurement error was considered insignificant.

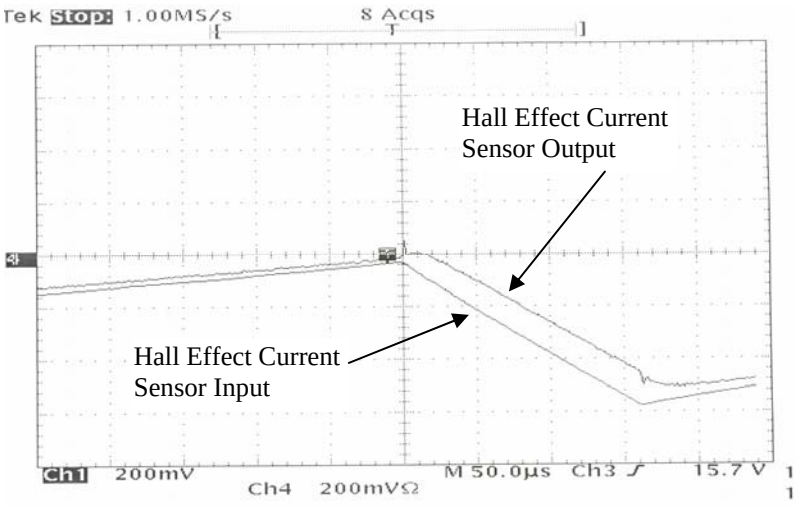


Figure 4.16: Measurement of Hall Effect current sensor delay

As stated earlier, the Hall Effect current sensor has a frequency range of DC to 25 kHz. However, the maximum frequency of 25 kHz can be misleading especially when monitoring output ripple current of inverters that employ hysteretic current control. To explain this, consider the rise and fall times of the switched current I_s of a unipolar hysteretic current control inverter shown in Figure 4.17. The minimum switching frequency is about 4.14 kHz and is well within the bandwidth of a 0 to 25 kHz current sensor. However, the rise time of 10.42 µs indicates the presence of frequencies well above the operation bandwidth of the current sensor.

The limits for harmonic currents injected into the grid network by inverters, are given in Table 3.3 (Chapter 3). For an example, in this project 4% of the inverter rated output current gives a maximum value of third harmonic I_{s3} of 0.236 A. From equation 3.41 in Chapter 3, the implementation delay t_d of 18 µs will produce I_{s3} of about 0.16 A. Similarly, it can be shown that using the existing current loop parameters (V_c =400V, V_s =240 V, L =10 mH, and $\hat{I}_s$ = 5.9 A), the levels of all the low frequency harmonics should be below the limit specified by AS4777.2, 2005. The delay t_d can be increased from 18 µs to a maximum delay of 25µs without exceeding

the upper limits. Therefore, to keep the cost of the inverter system down the existing Hall Effect current sensor will be used for the rest of this project.

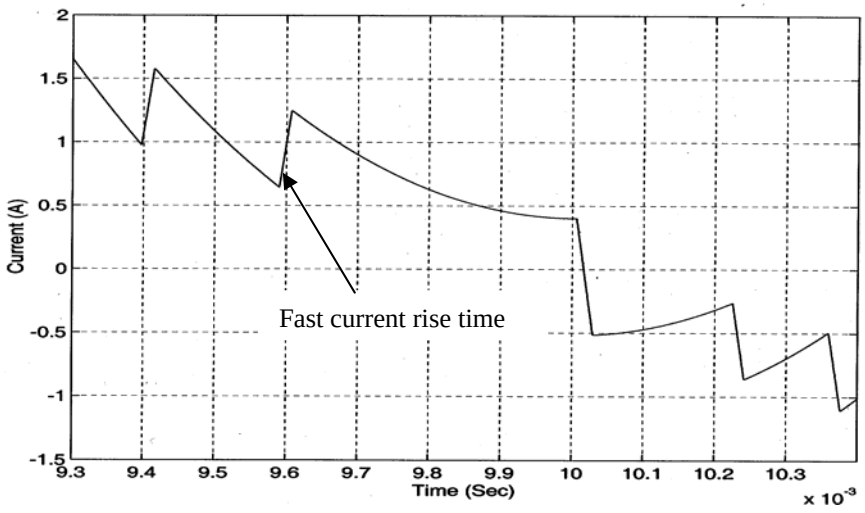


Figure 4.17: Rise and fall time of current I_s using SIMULINK

To experimentally validate the design procedure, the inverter output is connected via an earth leakage circuit breaker to the mains supply. Experimental results are shown in Figure 4.18 and the corresponding simulation result using 18 μs delay in the theoretical model of the current loop (Figure 3.14), yielded the results given in Figure 4.19.

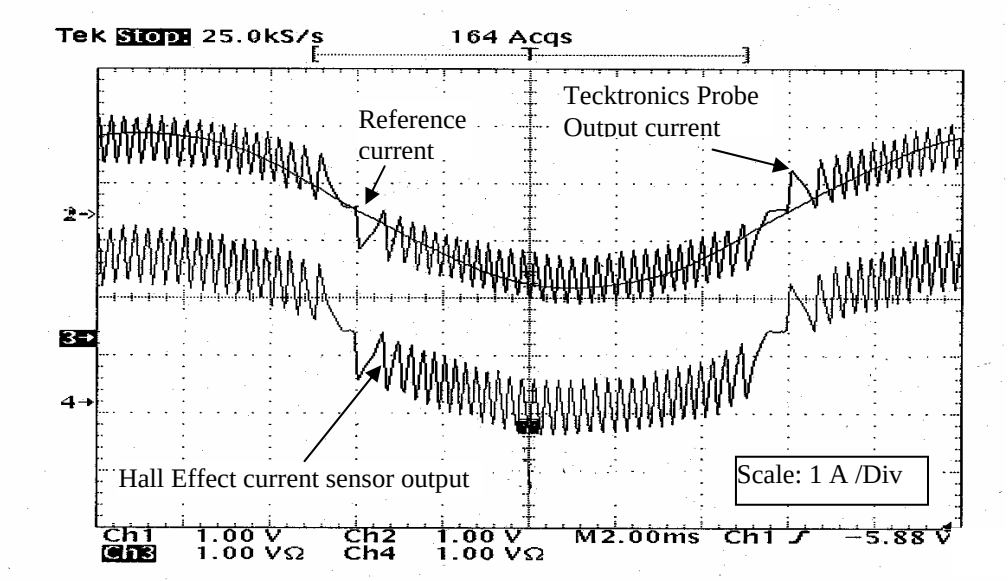


Figure 4.18: Experimental result of inverter output current without switching frequency filter

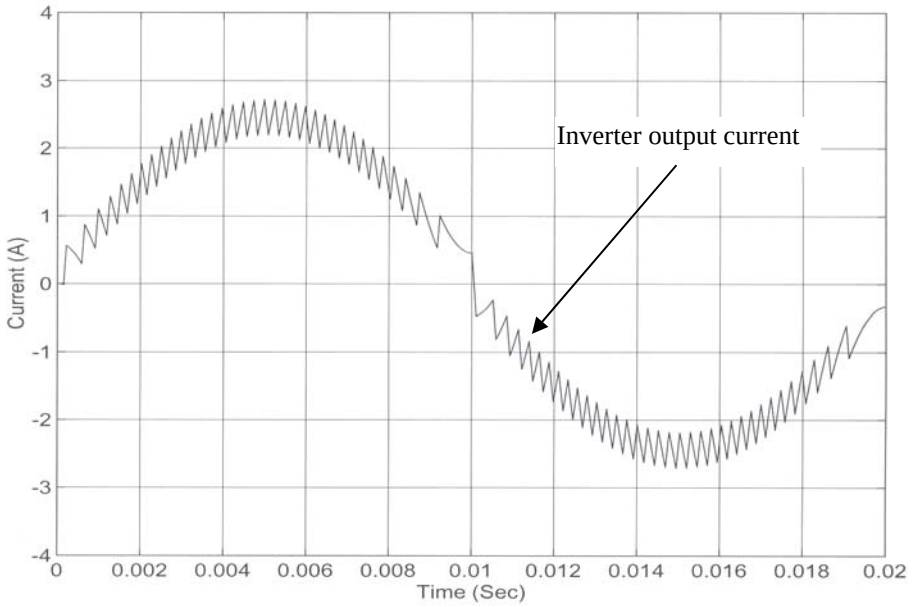


Figure 4.19: Simulation results of inverter output current using SIMULINK

The key switching frequencies F_{max}, F_{med} and F_{min} were also obtained using 18 μs for the experimental value of t_d in the current loop design equations 3.22 to 3.25 developed in Chapter 3. It was found that the difference in the values for F_{max} was in

the range of 3% to 5% for different values of the inverter output current. There was however, a difference of about 8% between the SIMULINK simulation results and the experimental results for the value of F_{med}. The largest difference of about 13% to 18% was between the experimental results and values for F_{min}.

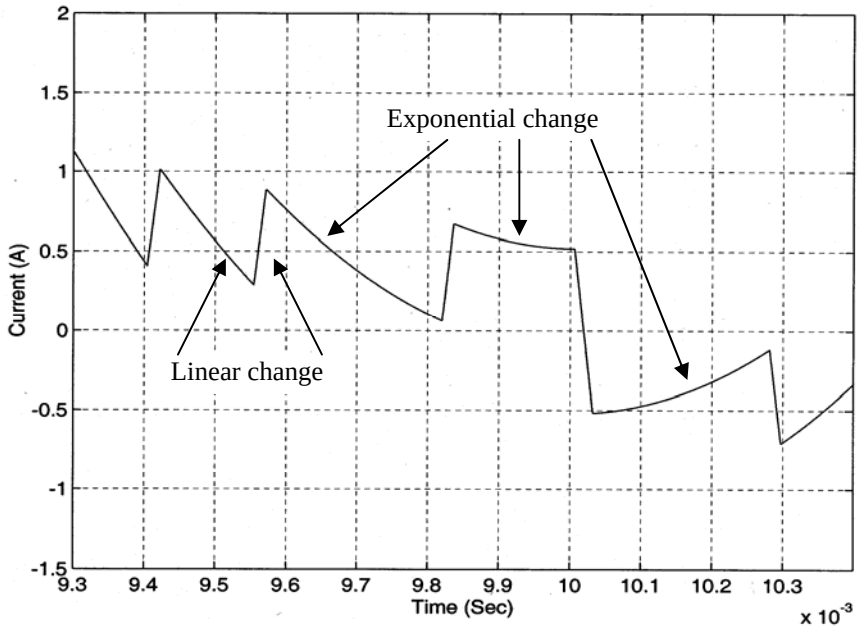


Figure 4.20: Switched current I_s near zero-crossing

The larger difference between the theoretical and experimental values for F_{min} is due to the following: -

- In the hysteretic current control switching model of the inverter bridge shown in Chapter 3 (Figure 3.3), it is assumed that the ripple current rises and falls linearly within the tolerance band (I_{Tol}). This assumption was based on the fact that the tolerance band chosen was very small compared to the magnitude of the rated current. However, with a delay of 18 μs the tolerance band becomes ineffective. It was shown in section 3.6, that tolerance band becomes ineffective if $t_d > \frac{I_{Tol}L}{V_c}$. In this case, for values chosen for V_c, L and I_{Tol}, the delay t_d should be less than 5 μs. Hence, the change in current with time is exponential for a period of about 0.8ms, as illustrated by Figure 4.20.

- It is difficult to measure exact values of inductances, capacitances, amplifier gains etc. Therefore instrumentation errors and skin effects need to be taken into account if greater accuracies are to be achieved.

Taking into account the large number of variables, and the assumptions made (e.g. source impedance ignored) when developing equations 3.22 to 3.25, the difference between the theoretical and experimental results of about 5% over most of the current waveform, and about 18% near the zero crossing, can be considered reasonable. The original assumptions used to develop the new design equations for the current loop in Chapter 3, can also be considered to be validated. While it was important to verify the accuracy of using the design equations to determine the current loop components, it is equally important to demonstrate the effect of excessive implementation delays on the inverter performance.

Large implementation delay will influence the ability of the current controller to keep the current within the tolerance band, and hence will lead to an increase in the magnitude of low frequency current harmonics injected into the grid system. Delay also limits a designer's ability to minimise the copper loss in the current loop.

To experimentally demonstrate that delay places a lower limit on the magnitude of the inductance of the current loop, the latter was reduced by 50%. Figure 4.21 shows the expected increase in switching frequency when compared to the results shown in Figure 4.17. Comparison with Figure 3.23 shows the same reduction in peak value, and existence of a pedestal, due to enhanced effect of circuit delay.

However, keeping the ratio of $\hat{V}_s$ to V_c at 0.9, also illustrates the expected increase in the distortion of the inverter output current and in the magnitude of current ripple (Figure 4.21). The tolerance band becomes ineffective and the current is no longer sinusoidal. With reference to equations 3.42 (Chapter 3), the distortion of the current can be reduced either by reducing the ratio of $\hat{V}_s$ to V_c, (increasing V_c) or by reducing

circuit delay. However, an increase in V_c will lead to an increase in switching losses, and is unacceptable if the aims of this project are to be achieved.

To demonstrate the impact of reducing the current sensor delay, the Hall Effect sensor (25 kHz bandwidth) was replaced by a Tektronics current probe with a bandwidth of 40 MHz. Improvement in the ability of current controller to follow the reference current when compared to the results shown in Figure 4.21 is illustrated by Figure 4.22. This experimental result confirms that delay limits the minimum inductance that can be used, if distortion of the inverter current is to be kept at acceptable levels. Hence implementation delay cannot be omitted from inverter design equations if these equations are to yield realistic current loop component values. This result also validates the theoretical relationship between delay and current distortion shown in Figure 3.23 (Chapter 3).

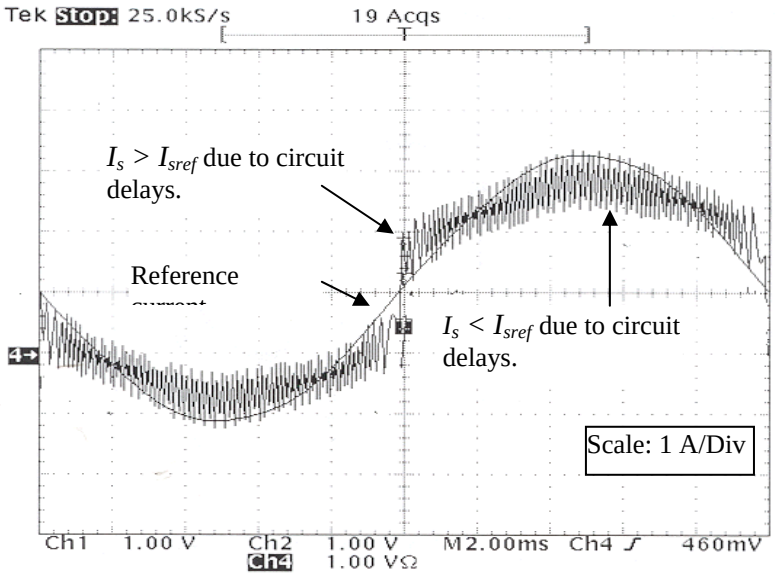


Figure 4.21: Current distortion using Hall Effect Current Sensor (delay 18 μs and inductance reduced by 50%)

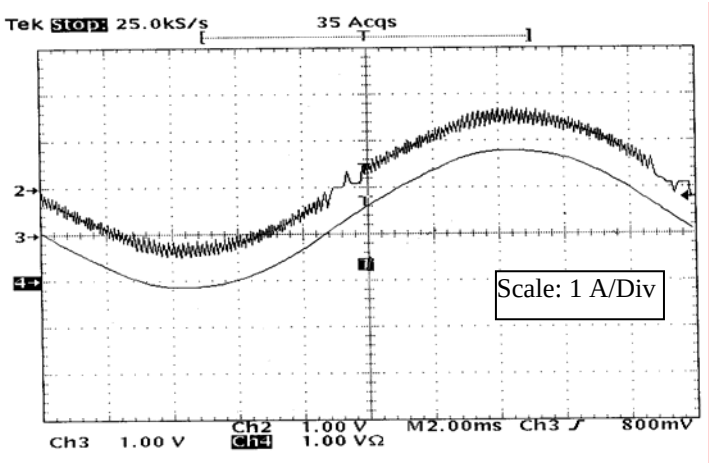


Figure 4.22: Using a Tecktronics Current probe as Current Sensor (inductance reduced by 50%)

While it has been shown that using the Tecktronics current probe (40 MHz bandwidth) can significantly reduce the magnitude of the tolerance band, and hence the current distortion, it is not an economical solution. The use of this current probe has however allowed the testing of the inverter to proceed.

The gate drive circuit delay of 2 μs was considered reasonable. However, the delay of 16 μs introduced by the circuit controlling switches T_{B+} and T_{B-} (Figure 4.5) had to be reduced to prevent unwanted switching, and current distortion near the zero crossing. This will be discussed in the next subsection.

4.5.1. Minimising Zero-Crossing Detector Circuit Delay

Further tests carried out on the circuit controlling leg B of the inverter-bridge revealed that a large percentage of the 16 μs delay occurred between the output of the voltage transformer and the output of the comparator TC1 shown in Figure 4.6. The main cause of this delay was the large time taken for the voltage waveform to change polarity at the zero crossing.

To improve the zero detecting process, the voltage from the transformer output voltage was first “clipped” using zener diodes and then amplified to give the results as shown in Figure 4.23. This minor change in circuit design resulted in a reduction

in the total delay of leg B by about 10 μs as illustrated by Figure 4.24. Blanking time between switching events at the zero crossing was also reduced from about 4 μs (Figure 4.13) to 1 μs. While a total delay of less than 2 μs would have been desirable, the new total delay of 4 μs was considered acceptable because this value of delay was unlikely to cause unwanted switching near the zero crossing.

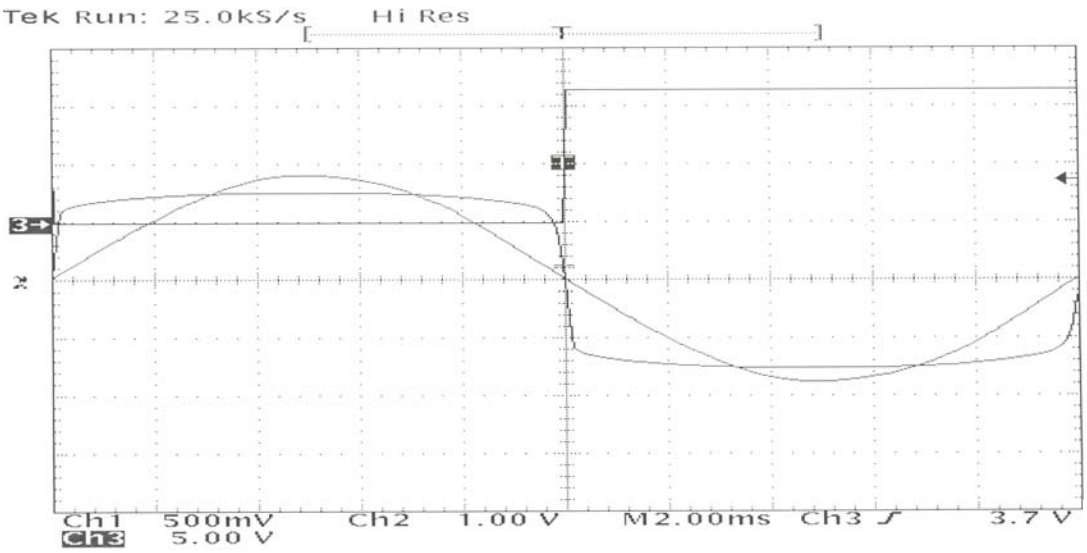


Figure 4.23: Voltage amplification results

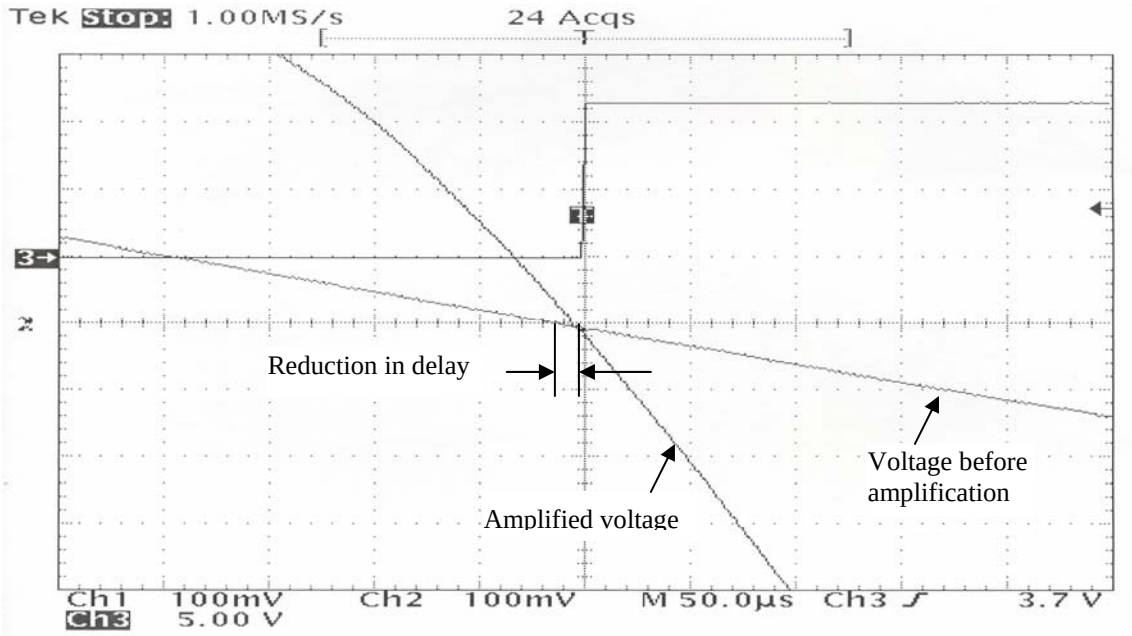


Figure 4.24: Reduction in zero detector delay

4.6. Conclusions

The circuits to implement the design for the current loop of the utility connected PV inverter system proposed for domestic applications, have been realised. The current loop test results (Figures 4.21 and 4.22) were obtained with the inverter output current fed to the grid supply.

The experimental results presented in this chapter demonstrate that the output of a unipolar switched inverter can be made less susceptible to its own switching noise by choosing the correct option from four equivalent switching options. It is a simple and cost effective method to overcome interference problems compared to methods such as, using constant frequency modulation, adaptively changeable hysteresis band methods and superimposing a common offset signal [33, 36-43] for bipolar inverters.

A split inductor arrangement (L_1 = 8 mH and L_2= 2 mH) has been used to minimise the influence of switching noise generated by the inverter bridge on the operation of other equipment connected at the PCC. The split inductor arrangement also removes the possibilities of unwanted switching near the zero crossing and hence prevents inverter failure.

Simple techniques have been presented to reduce circuit delays significantly and improve the performance of the inverter bridge. Of all the multiple steps to measure and process data, the Hall Effect sensor is the main source of delay. The measured total delay of 18 µs for leg B was well below 25 µs limit, and the level of low frequency harmonics generated by the inverter was also well below the limit specified by Australian Standard 4772.2, 2005. Therefore, there was no need to change the existing Hall Effect current sensor.

One of the stated objectives of this project is to improve the quality of the power supplied by the inverter system. In the next chapter the design of a cost effective switching frequency filter with negligible loss is presented.

CHAPTER 5

SWITCHING FREQUENCY FILTER DESIGN

5.1. Introduction

The current harmonics produced by the PV inverter system were discussed in detail in Chapters 2 and 3. Of these harmonics, the attenuation of the third harmonic will be included in the design of the voltage control loop (VCL) in Chapter 6. In this Chapter, a new design for a current loop filter network to remove switching frequency current harmonics from the inverter output current is proposed. This chapter is an expanded version of a paper presented by Sharma at AUPEC 2002 [63].

In Chapter 4, the initial filtering of the inverter output current was successfully achieved using the split-inductor arrangement (Figure 4.3). To minimise any additional power loss, it was decided to use this arrangement (i.e. no additional inductance) to form part of the inductance required for the switching frequency filter (SFF). It is shown in this chapter that filtering of switching frequency harmonics can be achieved by adding a capacitor and a resistor (to carry the ripple current) to this split inductor arrangement. The proposed filter design is not only cost effective but also has negligible power loss.

The following issues related to the switching frequency filter (SFF) arrangement are addressed:

- the design procedure of the SFF that yields component values of the filter
- the effect of the inclusion of the SFF on the stability of the current loop
- the effect of circuit delay on the performance of the SFF particularly near the zero crossing of the current waveform

- the effect of the SFF on the overall efficiency of the inverter system
- simulation results of the inverter current loop with the SFF

Experimental results to validate the theoretical design process of the SFF are also outlined in this chapter.

5.2. Design Methodology

The primary aim of the design process is to determine component values of the SFF to achieve maximum attenuation of the ripple current without introducing additional distortion or stability problems near the current zero crossing. To achieve these aims, the design of the SFF is carried out in two parts. In the first part the determination of the parameters of the filter based on the set of desired CCL specifications (e.g. the level of harmonic currents generated by the CCL should be below the limits given in Table 3.3 in Chapter 3), is carried out. Using the SFF component values derived from this theoretical exercise, the filter performance is analysed. This includes determining the magnitude and the phase response of the complete filter network.

To establish analytically if any interaction problems exist between the CCL and the SSF, is too difficult. Therefore, in the second part of this chapter, a SIMULINK model of the complete AC filter network is developed. This model of the filter is then incorporated into the current loop model developed in Chapter 3, and the performance of the current loop including the SFF is then evaluated.

5.3. Filter Design

Figure 5.1 shows the equivalent circuit model of the AC filter network. The main advantage of this filter network is that it achieves ripple current filtering or switching frequency filtering, without the need to increase the overall inductance and therefore the resistance of the output current loop. To further minimise the power loss of the current loop, the current magnitude tolerance band used in this application is small

(0.2 A) compared to $\hat{I}_s$ (5.9A) and hence the rms value of the ripple current is also small.

In Chapter 4, to keep the generation of low frequency harmonics within the legal limits [4], with the aid of equation 3.40 (Chapter 3), the total inductance was chosen as 10 mH. In the proposed modified filter network shown in Figure 5.1, the sum of the inductances of L_1 and L_2 is to remain unchanged at 10 mH. The inductance of L_2 is chosen to increase the impedance of the AC source such that at the switching frequencies (in the kHz range) Z_c provides a low impedance path for the ripple current. On the other hand, at the supply frequency of 50 Hz, the impedance Z_2 provides a low impedance path for the current I_s. Since the inductance of the mains supply is very much less than L, it has been ignored to simplify the SFF design process.

To avoid amplification of the ripple current the SFF components must be chosen carefully. The switching frequencies of the inverter IGBTs, near the zero crossing of the current I_s, must not coincide with the resonance frequency of the filter network. While the duration for which these two frequencies are equal may be brief, it can lead to large amplification of the ripple current. If this occurs near the current zero crossing then failure of the inverter bridge may occur. Theoretically, the magnitude of the tolerance band should limit the magnitude of the ripple current. However, as shown in Chapter 3 (equations 3.23 to 3.26), implementation delay t_d has significant influence on the switching frequency of unipolar switched inverters because the tolerance band becomes ineffective. Therefore for satisfactory performance of the SFF, its resonance frequency needs to be less than F_{min}.

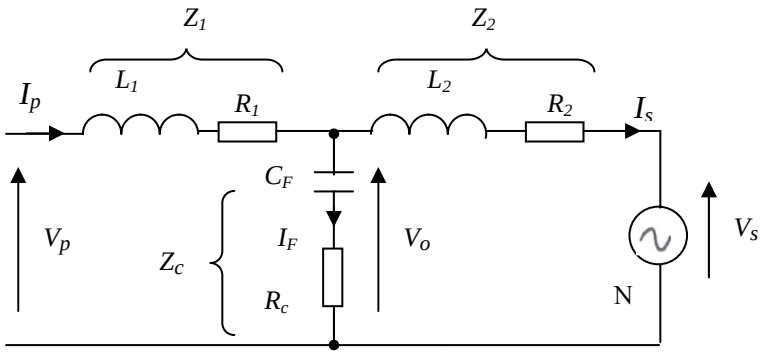


Figure 5.1: LCL ripple current filter

The capacitive reactance of the capacitor C_F has to be chosen such that phase displacement problems near the zero crossing are negligible. The phase displacement between the inverter output voltage and current may lead to an unacceptable level of distortion of the current, and improper switching of the inverter switches.

Theoretically, the use of the damping resistance R_c can be avoided because the magnitude of the ripple current is limited by the tolerance band. However, with delays of up to 18 μs, the current controller needs to be modified. This would be a complex and costly exercise. The use of R_c is a very cost effective method to limit the magnitude of ripple current, in the likelihood of the switching frequency coinciding with the ripple filter resonance. The value chosen for the damping resistor R_c is critical as it needs to: -

- provide adequate damping to prevent stability problems.

- ensure that the level of attenuation of the ripple current is maintained along the current waveform. If R_c is large it may lead to poor ripple current filtering at frequencies near F_{max}.

- ensure that SSF power losses are negligible.

As a first step in the design of the filter shown in Figure 5.1, knowledge of the inverter switching frequencies along a current cycle is required. Since the current loop parameters used in Chapter 3 will remain unchanged the switching frequencies obtained from Figure 3.6 (a) will be used. Therefore the values for F_{min} and F_{max} (when implementation delay was 10μs) were 2.95 kHz and 16.67 kHz respectively. The value of F_{min} is acceptable as it is greater than the value of 2 kHz suggested by Boys and Green [24]. To avoid distortion problems near the zero crossing, the values of L_1, L_2, R_1, R_2, C_F and R_c had to be chosen such that the resonance frequencies of the filter network were below F_{min} (2.95 kHz). The next phase in the design process is to determine the filter component values to meet these specifications.

At the switching frequency, equations 5.1 and 5.2 can be obtained applying Kirchhoff's to Figure 5.1.

$$Z_2 I_S = V_P \frac{Z_T}{Z_1 + Z_T} \tag{5.1}$$

where $Z_T = \dfrac{Z_c Z_2}{Z_c + Z_2}$

$$V_p = Z_1 I_p + Z_c (I_p - I_S) \tag{5.2}$$

The current transfer function denoted by equation 5.3, and obtained using equations 5.1 and 5.2, is a simple second order function.

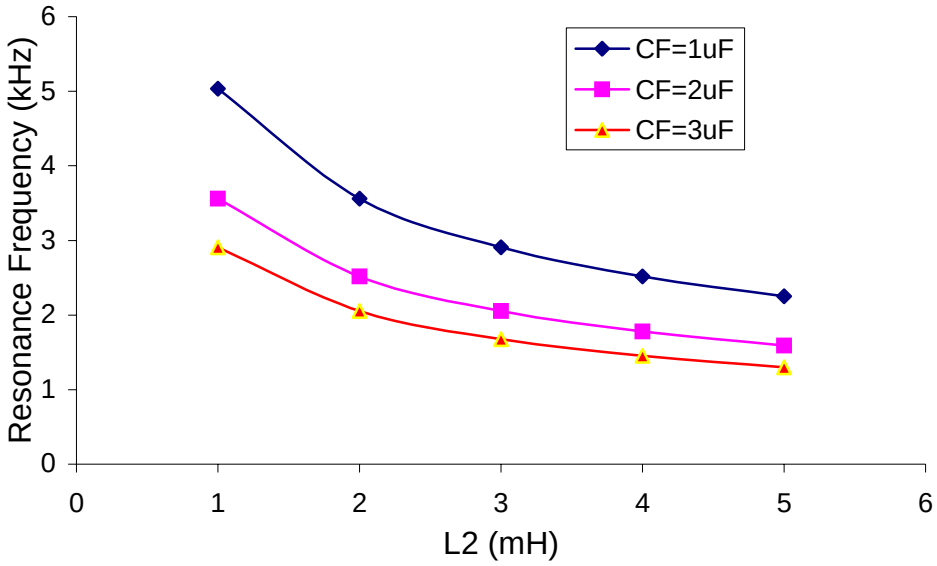
$$\frac{I_S}{I_p}(s) = \frac{sC_F R_c + 1}{s^2 C_F L_2 + s(C_F R_c + C_F R_2) + 1} \tag{5.3}$$

After division by $C_F L_2$, the denominator in equation 5.3 is of the form $(s^2 + 2\zeta\omega_o s + \omega_o^2)$ where,

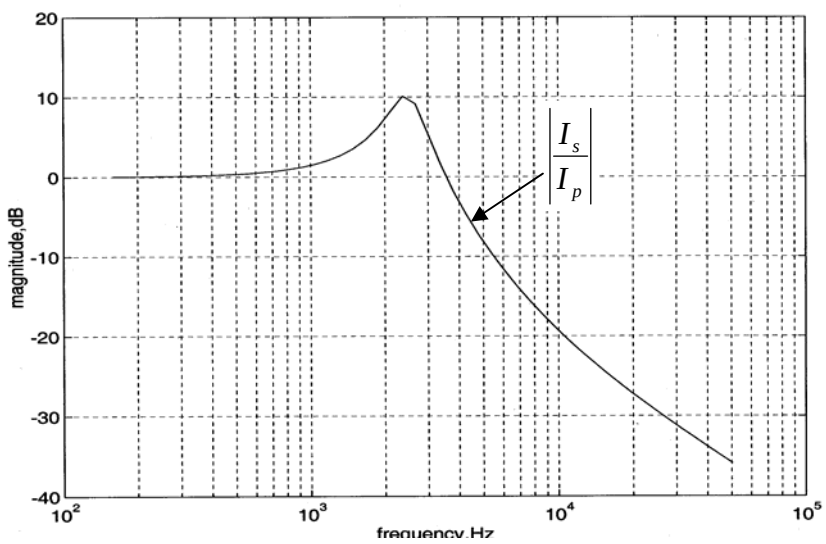
$$\omega_o = \frac{1}{\sqrt{L_2 C_F}} \qquad \text{and} \qquad \zeta = \frac{\left(R_c + R_2\right)}{2L_2\omega_o}$$

To ensure that the current loop power losses are minimised the resistance R_2 of the inductor L_2 is made as small as practically possible and is in the range of 0.1 Ω to 0.5 Ω. Since $R_2 << R_c$, the damping ratio ζ can be simplified to give $\zeta \approx \frac{R_c}{2}\sqrt{\frac{C_F}{L_2}}$. However, since hysteretic current control has been proposed, the maximum magnitude of the filter response (M_p) approximately given by $M_P = \frac{1}{2\zeta\sqrt{1-\zeta^2}}$ is of little significance if the resonance frequency (f_o) is less than F_{mim}. If f_o falls between F_{med} and F_{min}, amplification of the ripple current may occur as the two frequencies coincide leading to potential failure of the inverter bridge. As mentioned earlier, near the zero crossing, the tolerance band may be unable to limit the amplitude of the ripple current because of the effect of implementation delay.

To ensure that f_o is maintained below F_{min}, the values of L_2 and C_F chosen from the graph shown in Figure 5.2 (a), were 2 mH and 2 μF respectively. The capacitance of C_F should be as small as possible to allow the inverter to operate near unity power factor. The value of L_1 was therefore 8 mH to ensure that the total inductance of the current loop remained unchanged at 10 mH. The magnitude response of the SFF using these component values is given in Figure 5.2 (b) and the resonance frequency obtained from this curve is 2.516 kHz. Since f_o was less than F_{min} (2.95 kHz), the initial values chosen for R_c and R_2 were 5 Ω and 0.3 Ω respectively.



a) Choice of L_2 and C_F



b) Frequency Response

Figure 5.2: Resonance frequency of AC split inductor filter network
(L_2 = 2 mH, C_F = 2 µF, R_c = 5 Ω and R_2 = 0.3 Ω)

A SIMULINK model of the current loop was then developed and theoretical results for the inverter current loop with the SFF were obtained using these parameters.

5.4. Development of SIMULINK Model of Filter

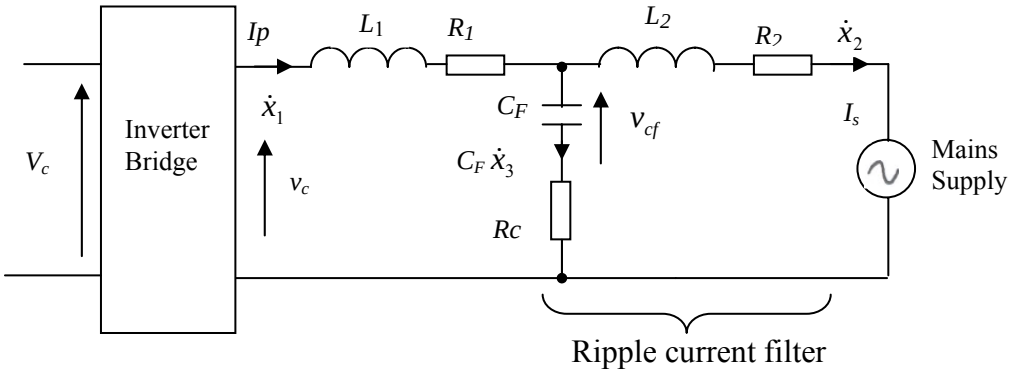


Figure 5.3 Inverter output with LCL ripple current filter

To develop a SIMULINK model of the complete AC filter network, consider the current loop model with the inclusion of the filter shown in Figure 5.3. The state equations 5.4 to 5.6 can be derived from this model of the filter network.

$$\dot{x}_1 = \frac{-(R_1 + R_C)}{L_1} x_1 + \frac{R_C}{L_1} x_2 - \frac{1}{L_1} x_3 + v_c \frac{1}{L_1} \tag{5.4}$$

$$\dot{x}_2 = \frac{R_C}{L_2} x_1 - \frac{(R_2 + R_C)}{L_2} x_2 + \frac{1}{L_2} x_3 \tag{5.5}$$

$$\dot{x}_3 = \frac{1}{C_F} x_1 - \frac{1}{C_F} x_2 \tag{5.6}$$

where $x_1 = i_p$; $x_2 = i_s$; and $x_3 = v_{cf}$

These three equations can be written in matrix form as illustrated by equation 5.7.

$$\dot{X} = \begin{bmatrix} (-R_1 + R_c)/L_1 & R_c/L_1 & -1/L_1 \\ R_c/L_2 & -(R_2 + R_c)/L_2 & 1/L_2 \\ 1/C_F & -1/C_F & 0 \end{bmatrix} X + \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \end{bmatrix} V_c \tag{5.7}$$

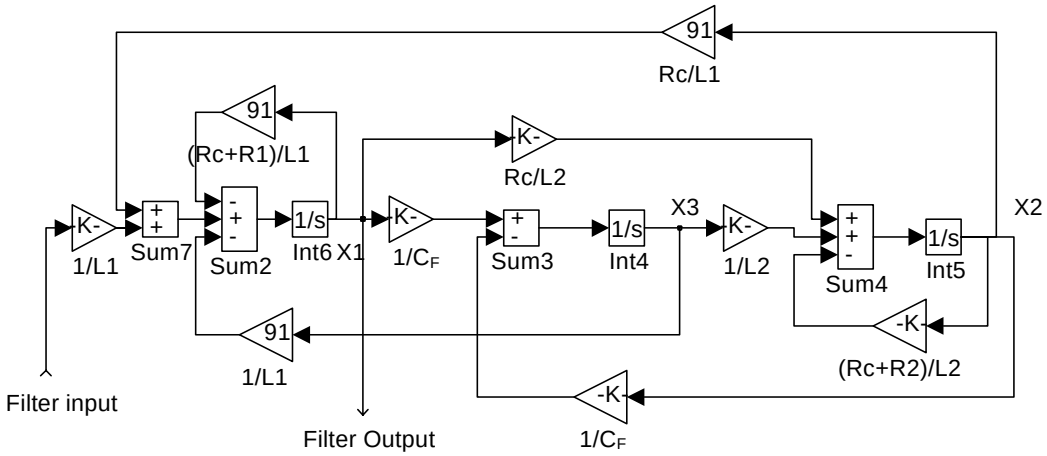


Figure 5.4: SIMULINK model of the complete AC filtering network

Using equation 5.7, a self-explanatory SIMULINK model of the filter network has been developed and is shown in Figure 5.4. In the next subsection the performance of the current loop using the SFF is analysed.

5.5. Simulation Results of Current Loop with Filter

The purpose of the simulation exercise was to determine the effectiveness of the split inductor filter network. This process was also necessary to establish if any interactions existed between the current loop and the filter network that would prevent them being designed separately. The SIMULINK model of the current loop with the SFF included is shown in Figure 5.5. This complete current controller model was developed by adding the split inductor filter model (Figure 5.4) to the current loop model shown in Figure 3.15 (Chapter 3). The assumptions used to develop the model in Figure 5.5 were the same as those used in section 3.3 (Chapter 3). The values of V_c, V_s and the rated current I_s were also the same values as those used in

Chapter 3. The values chosen for R_c, R_2, L_2 and C_F were kept the same as those used in section 5.3, that is, 5 Ω, 0.3 Ω, 2 mH and 2 μF respectively.

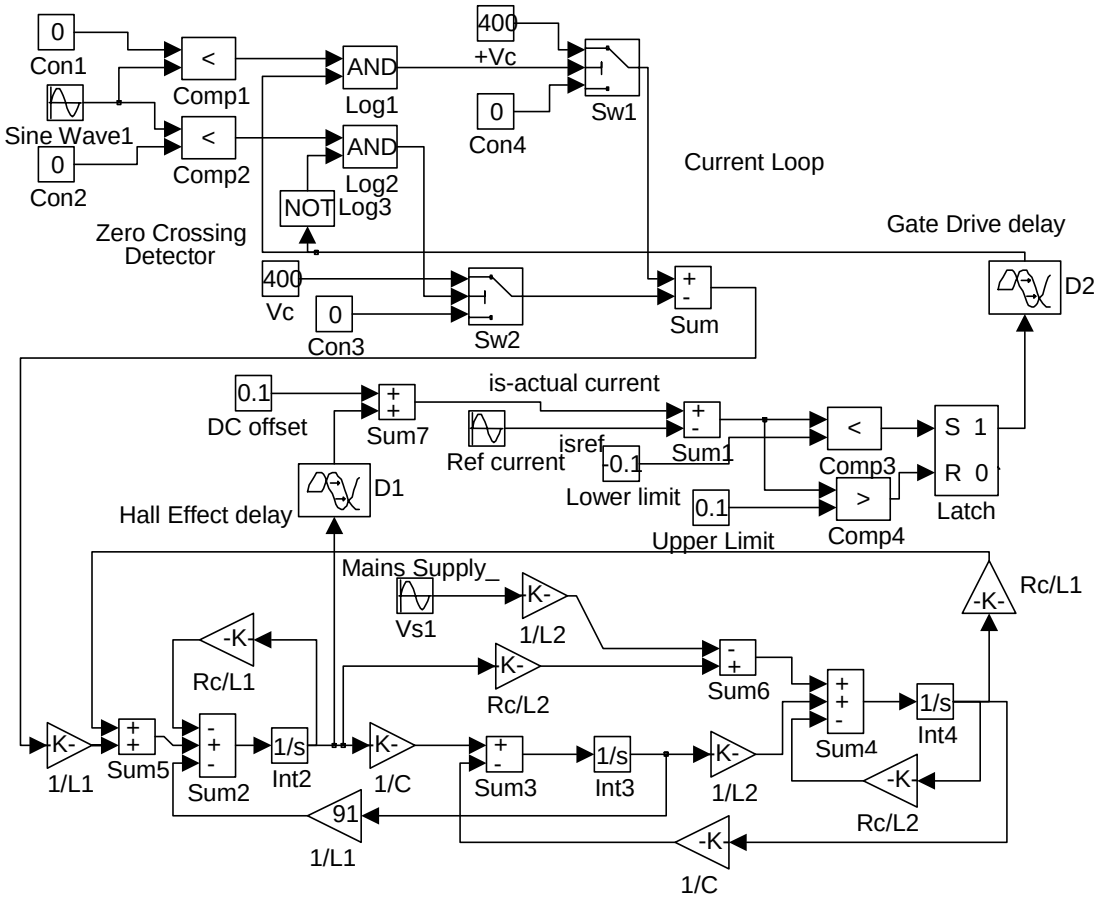


Figure 5.5: SIMULINK model of the current loop with switching frequency filter

The results of the unfiltered inverter output current is shown in Figure 5.6 and its corresponding FFT in Figure 5.7. These simulated results, when compared to the results of the inverter presented in Chapter 3, indicate that the addition of the new split inductor filter did not introduce stability problems.

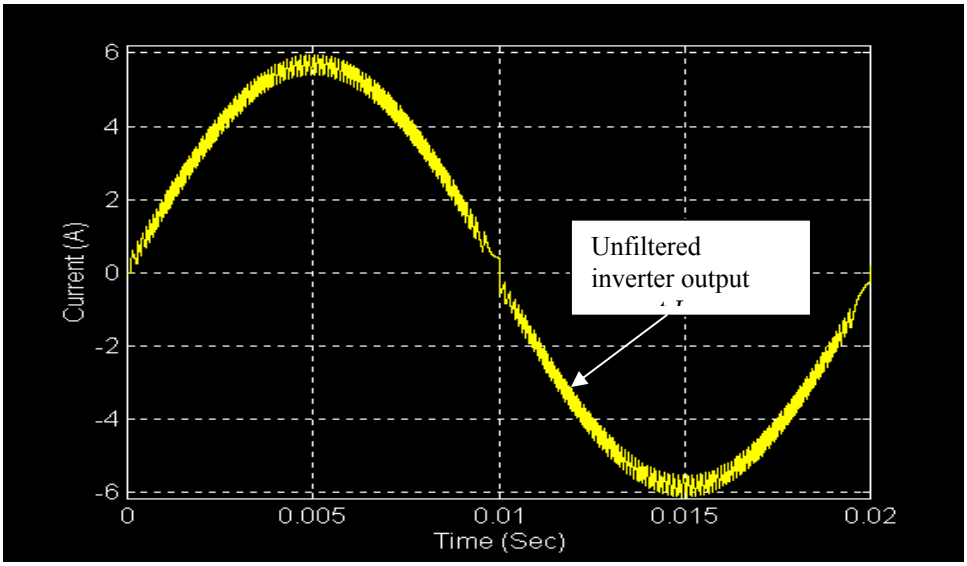


Figure 5.6: Inverter output current without switching frequency filter (t_d = 10 µs)

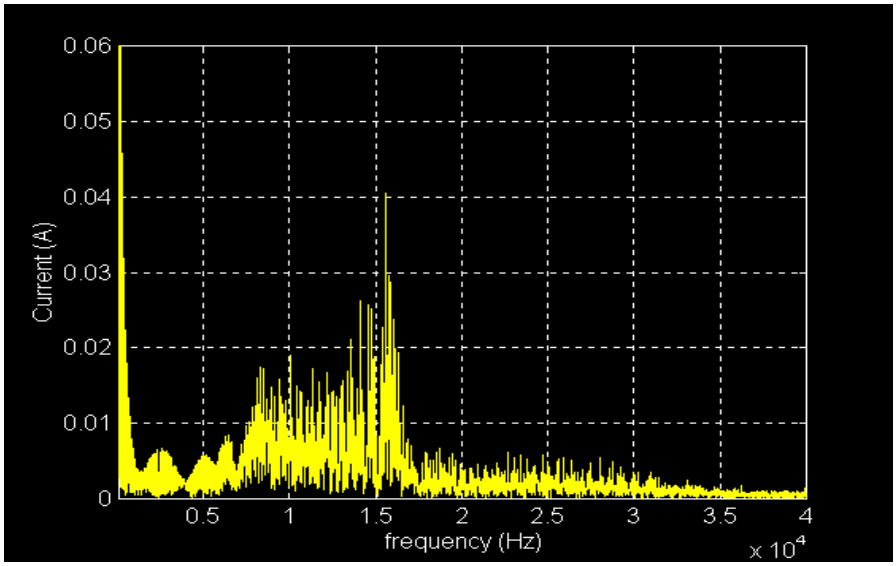


Figure 5.7: FFT of unfiltered current

The output of the SSF with the ripple current attenuated is shown in Figure 5.8. The corresponding switching frequency harmonics of the filtered current is illustrated in Figure 5.9. These theoretical results show that for a minor increase in cost (i.e. an additional capacitor and a resistor), the switching frequency harmonics can be almost totally removed, and the quality of the output current significantly improved. The

magnitude of the ripple current in Figure 5.10 indicates that power loss due to the filter is very small (less than 1 watt) and will not compromise the aims of this project.

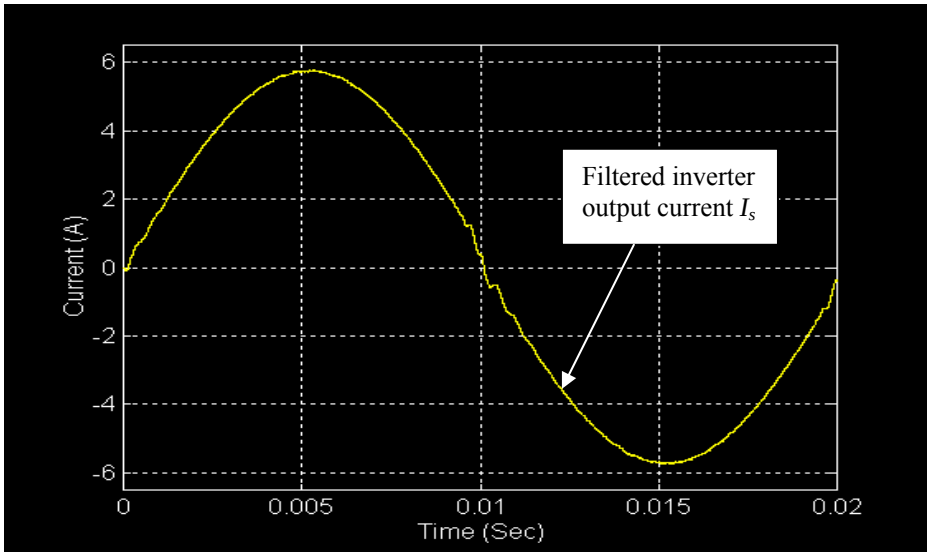


Figure 5.8: Inverter output current using switching frequency filter (L_1 =8 mH and L_2 =2 mH)

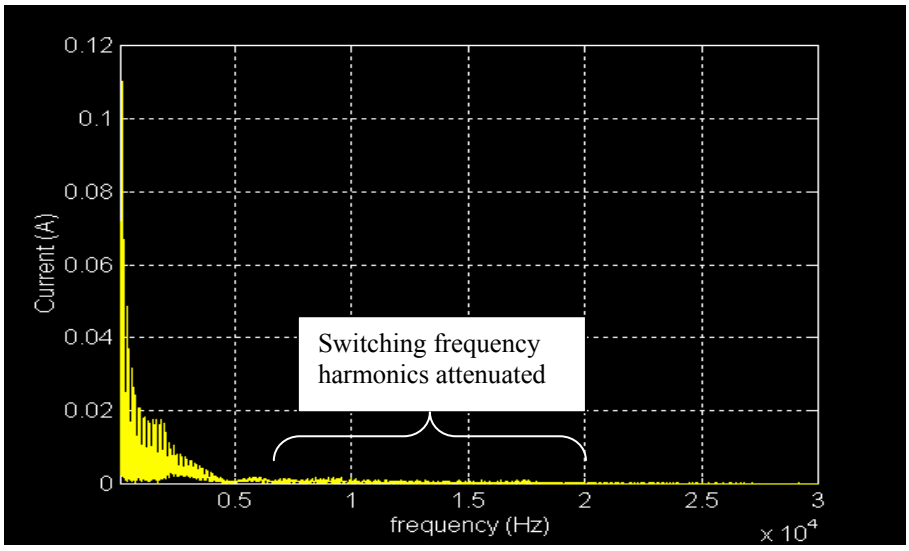


Figure 5.9: FFT of filtered output current

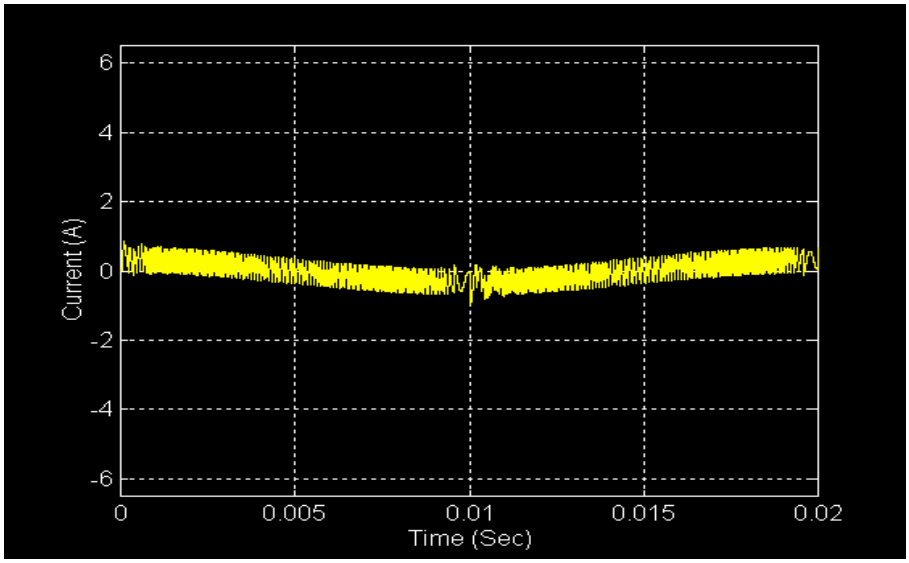


Figure 5.10: Ripple current through C_F and R_c

To demonstrate theoretically the importance of keeping the filter resonance frequency f_o less than F_{min}, the value of L_2 was reduced to 1 mH and L_1 increased to 9 mH. Since total inductance of the current loop remained unchanged at 10 mH, the switching frequencies over a current cycle remained unaffected.

The change in the ratio of L_1 to L_2 however, resulted in an increase in f_o from 2.516 kHz to 3.559 kHz (frequencies from Figure 5.2 (a)). Figure 5.11 shows an amplification of the ripple current, for a short duration, near the zero crossing. This increase in magnitude of the ripple current due to this increase in the resonance frequency ($f_o > F_{min}$), produced an increase in the level of current harmonics (Figure 5.12).

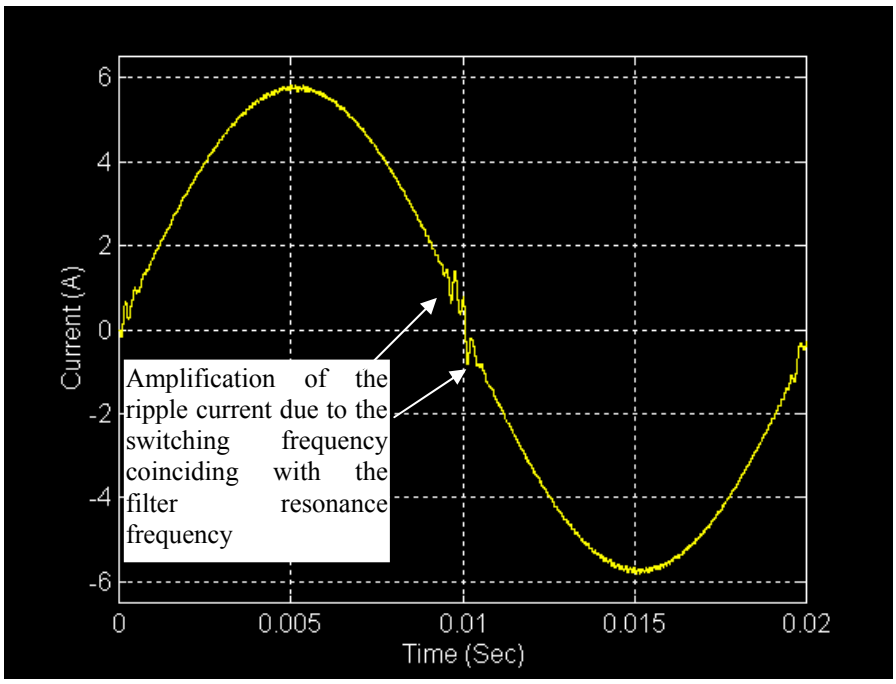


Figure 5.11: Output current when f_o > F_{min} (L_1 =9 mH and L_2 =1 mH)

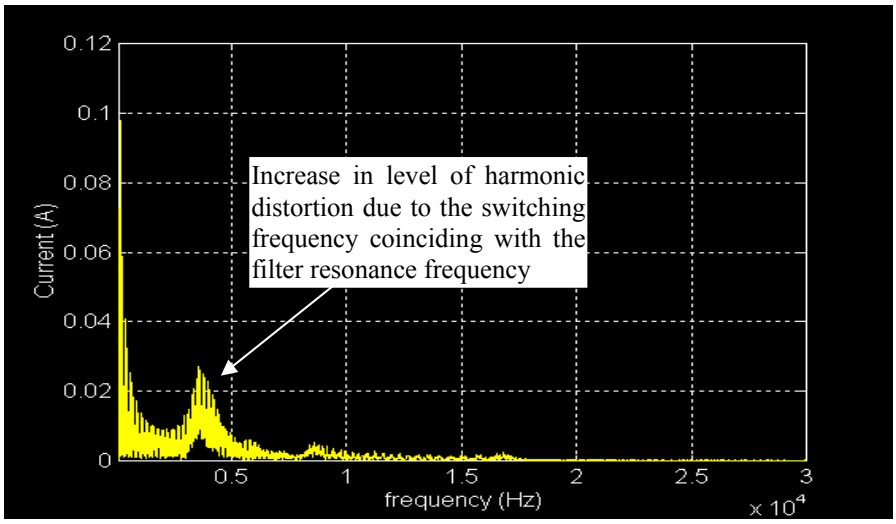


Figure 5.12: FFT of output current when f_o > F_{min}

It is obvious that increasing the value of the damping resistor R_c, for an example, from 5 Ω to 27 Ω will reduce the amplification of the ripple current near the zero

crossing as shown by Figure 5.13 and the corresponding reduction in the harmonics shown by Figure 5.14. The disadvantages of this approach however are the increase in the filter power losses and the small increase in magnitude of the switching frequency harmonics around F_{med} as shown by Figure 5.14. Therefore increasing the value of the damping resistor R_c may not be a viable option.

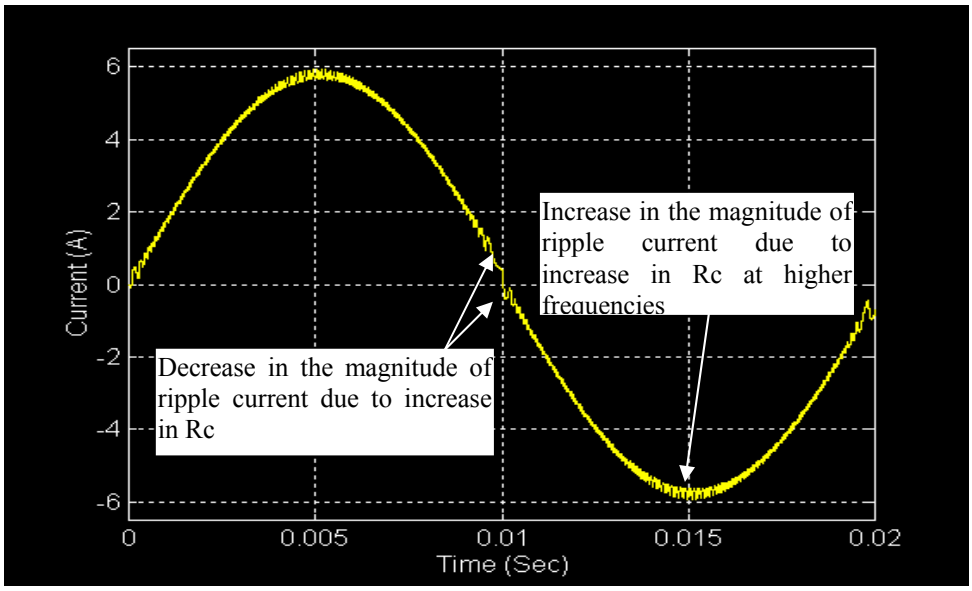


Figure 5.13: Effect of increasing R_c on magnitude of ripple current (L_1 =8 mH, L_2 =2 mH and R_c = 27 Ω)

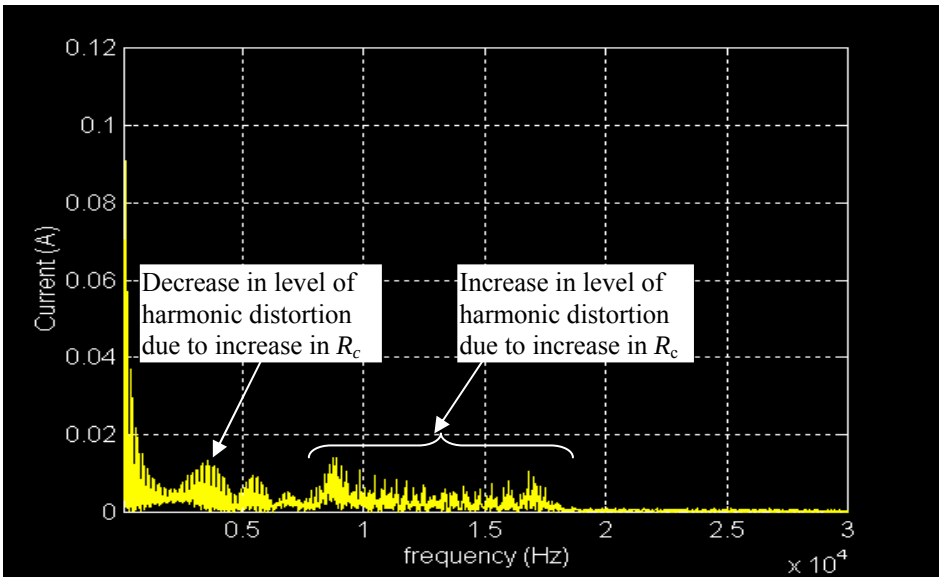


Figure 5.14: Effect of increasing R_c on level of current distortion (R_c = 27 Ω)

5. 5.1. Effect of reducing L1 and L2

In this subsection the effect of reducing the inductance and hence the resistance of the current loop on the quality of the SFF output, is investigated. Theoretically, this should improve the quality of the filtered output current I_s. However, the results shown in Figure 5.15 demonstrate that if L_1 and L_2 were reduced by 50%, (all other parameters of the current loop and filter unchanged), the magnitude of the ripple increases because the tolerance band is ineffective ($t_d . > \frac{I_{Tol} L}{V_c}$). Therefore, amplification of the ripple current occurs near the zero crossing occurs (Figure 5.16), because F_{min} decreases from 2.95 kHz to 2.1 kHz while f_o increases to 3.559 kHz.

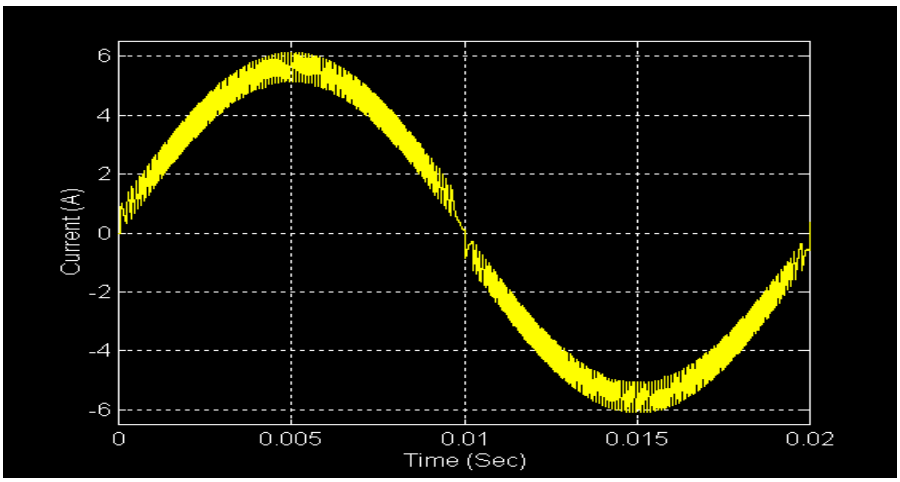


Figure 5.15: Tolerance band ineffective

The FFT of the filtered output current (Figure 5.17) shows an increase of about 5 times in the magnitude of current harmonics when f_o coincides with the switching frequency. Also, as shown in section 3.11.1 (Chapter 3), the odd harmonics generated by the CCL are given by $I_{s_n} \approx \left(\frac{t_d V_c}{2L} \right) \frac{4}{n\pi}$, and if L is halved then the low frequency harmonics will be approximately doubled. Therefore, if the inductance of the current loop needs to be changed, then other SFF parameters also need to be changed if the magnitude of current harmonics is to be maintained at a low level.

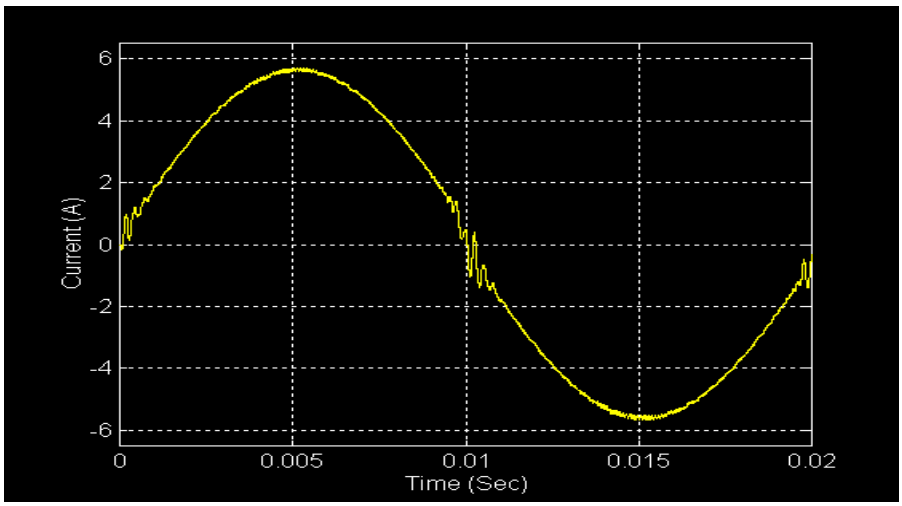


Figure 5.16 Increased current distortion near zero crossing (L_1 =4 mH and L_2 =1 mH)

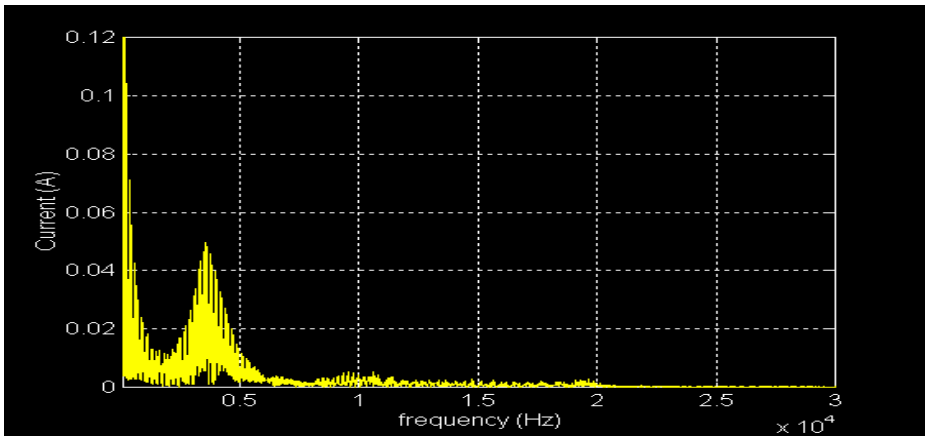


Figure 5.17 Effect of reducing L on output current

Finally, simulations of the current controller and the AC filter network revealed that the interactions between the two loops were insignificant and therefore each of these loops can be designed separately.

5.6. Experimental Results

Initially, the current loop parameters were deliberately chosen to force the resonance frequency f_o of the SSF network to coincide with firstly F_{min} and secondly with F_{med}. The aim of this exercise was to show experimentally the importance of maintaining f_o less than F_{min} for successful attenuation of the ripple current particularly near the zero crossing. Figure 5.18 illustrates the effect of f_o coinciding with the switching frequency near F_{min} and demonstrates the inability of the tolerance band to limit the magnitude of the ripple current. As stated earlier, this increase in the amplitude of the ripple current near the zero crossing can lead to unwanted switching resulting in the failure of the inverter bridge.

Figure 5.19 shows that if f_o is greater than F_{min} then this condition can also lead to problems when f_o coincides with switching frequencies near F_{med}. Therefore f_o needs to be less than F_{min} for successful operation of the SFF because the tolerance band may not be able to limit the magnitude of the ripple current due to implementation delay.

Performance analysis of the unipolar switched inverter using current loop and SFF components as close as possible to the theoretical design values in chapters 3 and section 5.4 was carried out. When the actual values of the filter components were measured, they were found to be:

$C_F = 2.22\ \mu F$

$R_c = 5.08\ \Omega$

$L_1 = 8.34$ mH

$L_2 = 2.2$ mH

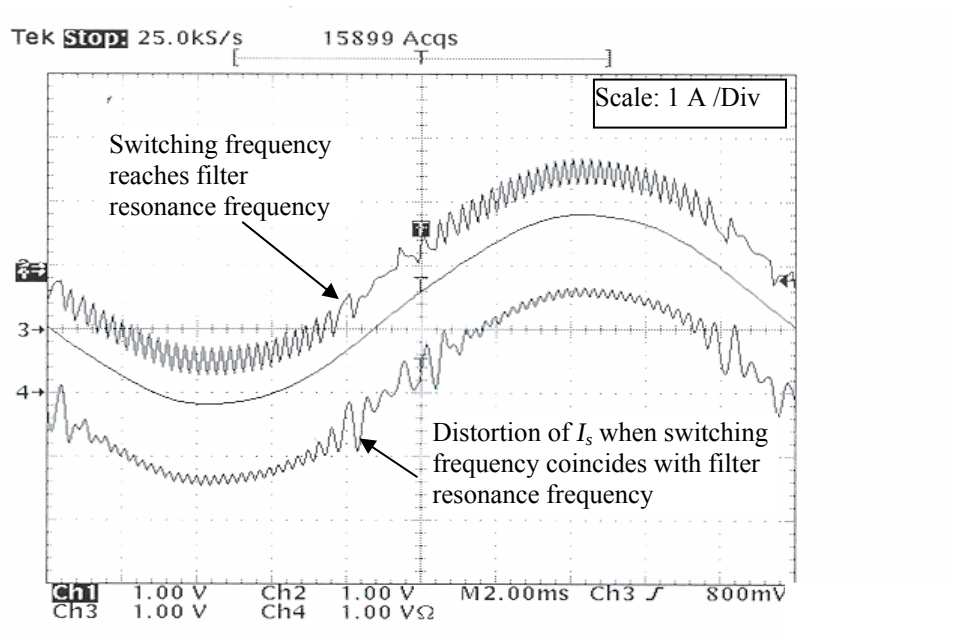


Figure 5.18: Filtered inverter output current when f_o coincides with F_{min}

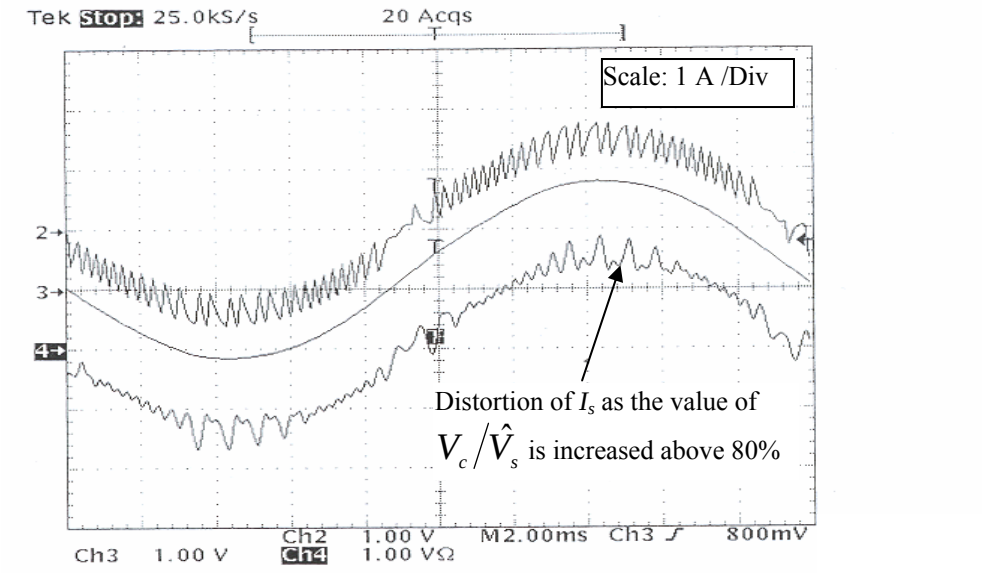


Figure 5.19 Filtered inverter output current when f_o coincides with F_{med}

Experimental results for the inverter supplying about 500 W of power to the grid system using the current loop and the SSF parameters from the theoretical analysis are shown in Figures 5.20 and 5.21. These results demonstrate the excellent ripple current filtering properties of the new SSF and validate the filter design process. The results agreed with the simulations results shown in Figure 5.8. Additional results are included in Appendix E to demonstrate the effect of delay on the filtered inverter output current.

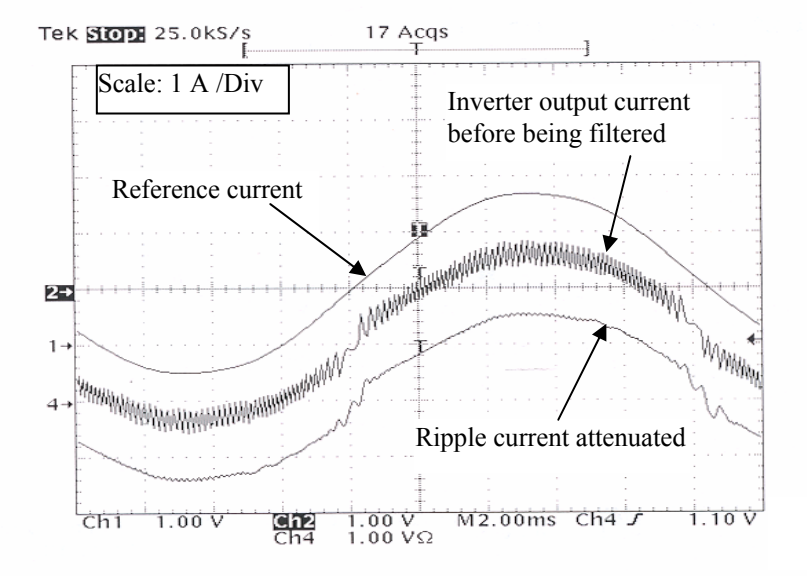


Figure 5.20: Inverter supplying power to grid system

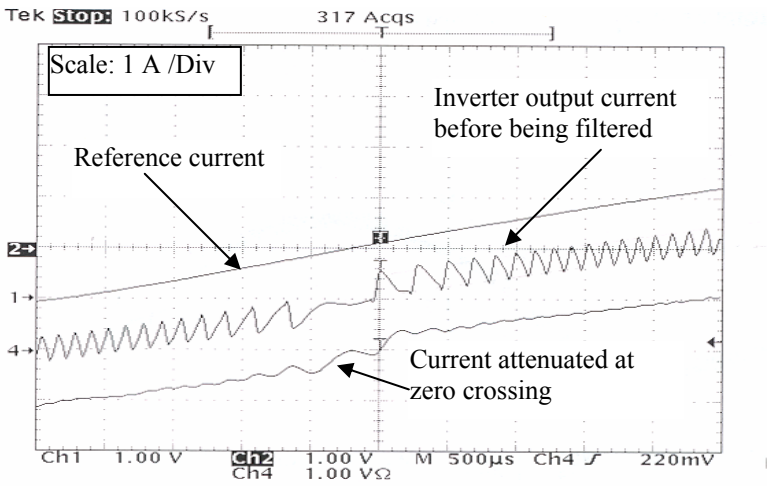


Figure 5.21: Improved attenuation of ripple current near zero crossing

5.7. Conclusions

The theoretical results obtained for the performance of the current loop with the new SFF presented in this chapter show that: -

- the stability and the performance of the current loop are unaffected by the new split inductor AC filter network as long as the filter resonance frequency is maintained less than the F_{min} of the inverter switches. This can be easily achieved by choosing appropriate values for L_1, L_2, C_F and R_c.

- filtering of the switching frequency harmonic currents can be achieved without sacrificing the overall conversion efficiency of the inverter system

- the removal of the switching frequency current harmonics using the proposed split inductor filter arrangement is a very cost effective method to use. Only two additional components, a capacitor, and a resistor to divert the small ripple current are required.

- the circuit propagation delay is an important variable that influences the efficiency of an inverter system.

These conclusions have been achieved by assuming that the current control loop (VCL) was perfect. In the next chapter the interactions between the VCL and the CCL and the effects of the third harmonics generated by the VCL are investigated.

CHAPTER 6

VOLTAGE LOOP: P-CONTROLLER VERSUS PI-CONTROLER

6.1. Introduction

The power losses associated with a voltage controller are very small compared to those in the current loop. Its performance however, is important if the level of third harmonic currents injected into the grid system is to be maintained below 4% of the fundamental value as specified by the Australian standard 4777.2, 2005. The control of the DC input voltage (V_C) is also important as it influences switching losses.

In applications where a constant DC voltage is required, a proportional-integral (PI) controller, with its zero steady state error, is the obvious choice. However, for the PV applications being considered, the inverter DC input voltage regulation can be relaxed slightly. This was demonstrated in Chapter 4, where a change in DC input voltage of 30 V had little effect on the level of low frequency harmonics. Therefore, the suitability of a proportional (P)-controller required investigation.

The relationship between low frequency current harmonics, unipolar switching and implementation delays has been presented in Chapters 3 and 4. However, the contribution of low frequency current harmonics by the voltage controller was ignored. The product of the 100 Hz ripple (present in the input DC voltage) and the attenuated 50 Hz mains voltage gives rise to third harmonics. These third harmonics have the potential to add to those generated by the CCL and increase the total harmonics injected into the grid above the 4% limit. Therefore, in this chapter, the levels of current harmonics generated by the two types of controllers are analysed, before the preferred controller can be chosen.

The need to design a suitable voltage control loop (VCL), such that all the power developed by the PV generator is transferred to the grid supply, was discussed in chapter 2. Failure of the VCL to maintain this balanced power condition may cause the inverter system to malfunction due to an '*over or under input DC voltage'* condition and/or introduce unacceptable levels of distortion of the AC current. The voltage controller to be chosen has to respond to transients caused by not only AC mains supply voltage sags of up to 20%, but also to frequent changes in V_C due to cloud movement. Hence, dynamic and steady state analyses of the response of both types of controllers to these conditions are also presented in this chapter.

The research outcomes presented in this chapter include: -

- development of a theoretical model of the VCL that leads to minimum switching losses and minimum low frequency harmonic currents
- an evaluation of the performance of the VCL using both the P-controller and the PI- controller
- the performance of the VCL when subjected to changes in the DC input current i_y and the supply voltage V_s
- identification of any interactions between the current and voltage loops that may prevent the two loops being designed separately

6.2. Assumptions

To carry out a theoretical stability analysis of the voltage controller, the system is linearised and simplified to a second order system. To develop a simplified model of the voltage control loop, irrespective of the type of controller used, it is necessary to make the following assumptions: -

- that the current loop is perfect, that is, i_s instantaneously follows i_{sref}.

- that the mains supply voltage V_s is a noise free sinusoidal wave with a constant magnitude and therefore the time constant τ_{fa} of filter B (Figure 6.1) is assumed to be negligible
- that the non-linearities of the multiplier shown in Figure 6.1 are ignored

It will be shown that these assumptions are acceptable and do not have potential practical consequences.

6.3. Voltage Control Loop (P-Controller)

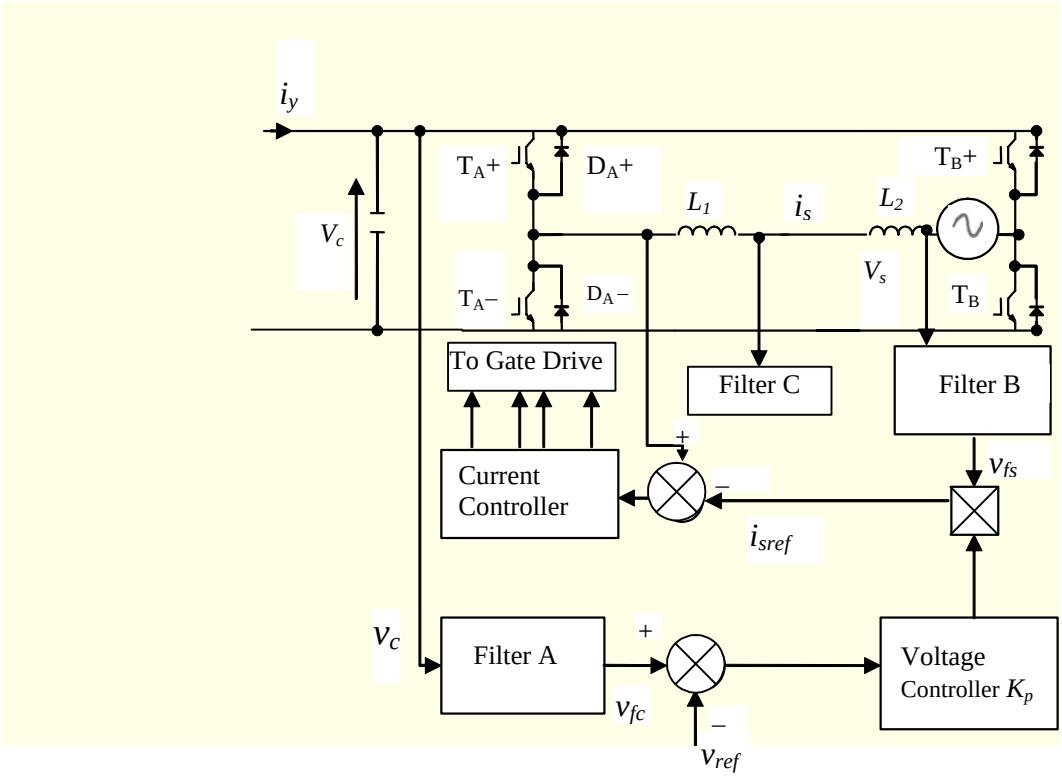


Figure 6.1: Inverter current and voltage controllers

In control terms, the normal operation of the inverter together with capacitor *C* may be considered as a two-input single output system. The inputs are i_y and v_{ref} (Figure 6.1) and the output is the capacitor voltage v_c.

A simplified block diagram of the voltage control loop using the P-controller is shown in Figure 6.2. The main function of the low pass filter A is to remove the dominant 100 Hz ripple component of the feedback voltage v_{fc}. Therefore, as a compromise between phase shift and harmonic rejection, the time constant τ_{fc} of this filter is chosen to be 0.05 s. The error voltage, which is the difference between v_{fc} and v_{ref}, is amplified by the proportional controller and multiplied by v_{fs}, which is a sine wave proportional to the line to neutral voltage v_s

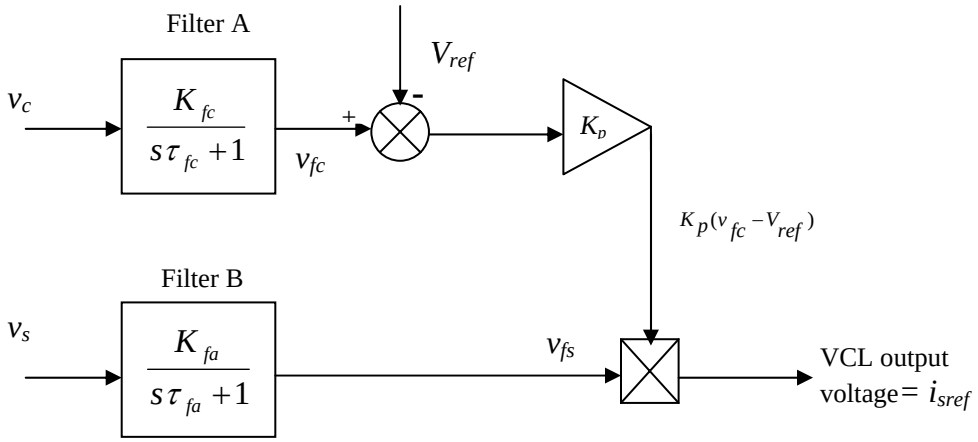


Figure: 6.2: Simplified VCL with P-controller

Low pass filter B reduces the high frequency content of v_{fs}. The output of the multiplier is a sinusoidal voltage in phase with the supply voltage v_s and has a magnitude equal to the reference current i_{sref}. Similarly, the output of the Hall Effect Current sensor in Figure 6.1 is also a voltage that is proportional to the current i_s. The current controller (Figure 6.1) provides switching signals for the inverter power electronic switches so that i_s is forced to stay within a small tolerance band around the reference current i_{sref}. For correct operation of the inverter, the DC input voltage V_c must be greater than the peak value ($\sqrt{2}V_s$) of the AC supply voltage (v_s). The value of V_C and those of inductances L_1 and L_2 were carefully chosen in Chapter 4 to minimise the switching frequency harmonics in i_s. If those harmonic currents are

ignored then i_s is approximately equal to i_{sref} and this equality is assumed in the analysis which follows.

The voltage control loop is designed such that if v_c rises above a desired value, then the rms value of i_s will rise. This causes more power to flow out of the inverter resulting in a drop of the capacitor voltage. Similarly if v_c falls below the desired value, then the rms value of i_s will fall causing a reduction in power flow from the inverter.

Since v_{fs} is forced to stay in phase with v_s, the power factor at the inverter output terminals is unity. While filter B is used as a zero phase shift filter, it can be easily adjusted to give a phase shift to allow the inverter power factor to be made adjustable. This facility would help improve the AC supply voltage regulation. However, for the reasons given in Chapter 2 this feature of the inverter will not be used in this project.

The equations derived for the VCL with a P-controller presented in this subsection were first published by Sharma in AUPEC 1992 [64]. However, this paper did not include analysis of the VCL with a PI-controller, and SIMULINK models of the VCL to determine the third harmonics generated by the two types of controllers.

The following power balance equation may be written for the capacitor in Figure 6.1:-

$$\frac{C}{2}\frac{d}{dt}\left(v_c^2\right) = i_y v_c - v_s i_s \tag{6.1}$$

Since the time constant of filter B, τ_{fa} (Figure 6.2) is assumed to be zero, equations 6.2 and 6.3 can be used to describe the voltage control loop.

$$i_S = K_p (v_{fc} - V_{ref}) v_S K_{fa} \tag{6.2}$$

$$\tau_{fc} \frac{d}{dt}(v_{fc}) + v_{fc} = K_{fc} v_c \tag{6.3}$$

Combining equations, (6.1) and (6.2) gives:

$$\frac{C}{2}\frac{d}{dt}\left(v_c^2\right) = i_y v_c - \left\{K_p K_{fa}(v_{fc} - V_{ref})v_s^2\right\} \tag{6.4}$$

Neglecting any ripple in i_y, at steady state, equations (6.2) and (6.3) can be used to give:

$$I_s = K_p K_{fa}(K_{fc}V_c - V_{ref})V_s \tag{6.5}$$

At steady state if all the power produced by the PV generator is transferred to the grid network, equation 6.1 can be simplified to give equation 6.6:

$$I_y V_c = I_s V_s \tag{6.6}$$

Combination of equation (6.5) and (6.6) yields: -

$$V_c = (V_{ref} / K_{fc}) / (1 - I_y / K_p K_{fc} K_{fa} V_s^2) \tag{6.7}$$

Equation 6.7 allows the steady state value of V_c to be estimated as the input current I_y increases. As expected, equation 6.7 also indicates that for a P-controller the steady state error in V_c will increase as i_y increases from zero to its rated value. Therefore the gain product $K_p K_{fc} K_{fa}$ must be large enough to ensure that the steady state error in V_c does not become excessive at the rated value of I_y.

Another consideration is the transient response of the VCL due to changes in input current i_y. Analytical solution of equations 6.1 to 6.5 is difficult because the term v_c^2 in equation 6.1 makes it non-linear. However, some insight into the problem of selecting values for the control system parameters may be obtained by linearising these equations about a steady state operating value.

Linearisation of equation 6.1 is carried out as shown.

$$C(V_c + \Delta v_c)\, d(V_c + \Delta v_c)/dt = (I_y + \Delta i_y)(V_c + \Delta v_c) - V_s(I_s + \Delta i_s) \tag{6.8}$$

Since the term $(\Delta i_y \Delta v_c)$ in equation 6.8 is very small, it can be neglected. Also the term $\frac{d}{dt}V_c$ equals zero because V_c is a steady state value. As the inverter bridge losses are neglected it can therefore be assumed that $I_y V_c = I_S V_S$ and equation 6.8 becomes:

$$CV_c \frac{d}{dt}(\Delta v_c) = \Delta i_y V_c + I_y \Delta v_c - V_s \Delta i_s \tag{6.9}$$

Since V_{ref} is preset at a fixed value, Δi_S can be obtained using equation 6.2: -

$$\Delta i_S = K_p K_{fa} \Delta v_{fc} V_s \tag{6.10}$$

Combining equations 6.9 and 6.10 gives: -

$$C\frac{d}{dt}(\Delta v_c) = \Delta i_y + (I_y \Delta v_c)/V_c - (K_p K_{fa} V_s^2 \Delta v_{fc})/V_c \tag{6.11}$$

In equation, 6.11 ‘Δ’ represents small deviations of all the variables about their corresponding steady state values. The deviation and the rates of change of Δi_s and ΔV_{fc} are assumed to be small compared to I_s and V_{fc}. Changes in insolation level and /or temperature results in a change in current i_y which is represented by Δi_y in equation 6.11

Using equation 6.3 to substitute for Δv_{fc} and taking the Laplace transformation of equation 6.11, gives a second order function with a zero.

$$\frac{\Delta v_c}{V_c} = \frac{K(s\tau_{fc}+1)\Delta i_y}{(s\tau_{fc})^2 + s\tau_{fc}[1-KI_y] + K(K_p K_{fa} K_{fc} V_s^2 - I_y)} \tag{6.12}$$

where $K = \tau_{fc} / CV_c$

The denominator of equation 6.12 is of the standard second order form: $s^2 + 2\zeta\omega_0 s + \omega_0^2$

Where $\omega^2{}_0 = \frac{1}{CV_c\tau_{fc}}\left[K_p K_{fa} K_{fc} V_s^2 - I_y\right]$ and $\zeta = \left[\frac{1-KI_y}{2\sqrt{K}\sqrt{K_p K_{fa} K_{fc} V_s^2 - I_y}}\right]$

Since V_s is fixed by the supply authority, the values of both ω_0 and ζ will depend on the value of the gain product $\left(K_p K_{fa} K_{fc}\right)$. In practice, $K_p K_{fc} K_{fa} V_s^2 >> I_y$ and $KI_y << 1$, therefore, the changes in the solar panel output current I_y will have insignificant effect on ω_0 and ζ.

If Δi_y is a unit step function, then in the time domain equation 6.12 becomes: -

$$\frac{\Delta v_c}{V_c} = \left[\frac{1}{(K_p K_{fa} K_{fc} V_s^2 - I_y)} + \frac{K(1-a)e^{-at/\tau fc}}{a(a-b)} + \frac{K(1-b)e^{-bt/\tau fc}}{b(b-a)}\right] \tag{6.13}$$

where $a, b = (1-KI_y)/2 \pm \left((KI_y - 1)^2/4 - K(K_p K_{fc} K_{fa} V_s^2 - I_y)\right)^{1/2}$

The aim of the analytical work so far has been to obtain suitable values of K_p, K_{fc} and K_{fa}, such that the steady state error and the settling time of V_c (due to changes in i_y) are within predetermined values. However, it is also important to note that V_c (and therefore V_{fc}) has a dominant harmonic at twice the supply frequency. The presence of this harmonic, gives rise to a third harmonic in i_s whose magnitude will be estimated in section 6.7.

If the value of K_p is chosen is too small then the control loop will behave like an overdamped system, with a large steady state error in V_c giving rise to an increase in switching losses. On the other hand, if in the attempt to make the steady state error very small, K_p is made very large then V_c may oscillate with constant amplitude or in the worse scenario the amplitude may rise exponentially creating a dangerous situation. Therefore, K_p needs to be chosen so that the steady state error is acceptable, that is, any increase in switching losses is negligible, and the control system response will behave like a slightly underdamped second order system. Also, K_{fc} and K_{fa} need to be chosen such that during implementation, the operational amplifiers used are not operating in the saturated region during normal operation.

Since the supply rail for the operational amplifiers will be ±12 V, it was decided that 0.02 would be a reasonable value for K_{fc} and for K_{fa} to commence simulation of the inverter bridge. The values for L, V_c, and V_s were kept the same as the values used during the current loop design process in Chapter 3 (V_c = 400 V, V_s = 240 V and L = 10 mH). By substituting the above values in equation 6.7, the value of K_p can be obtained for a given steady state error. For a steady state error of 10 V (at rated current), K_p was found to be 4.45.

Figure 6.3 shows a self-explanatory SIMULINK model of the VCL (P-controller) shown in Figure 6.2. A step change in the input current i_y from zero to 2.5A (rated current) was applied to the inverter and the response of the VCL is shown in Figure 6.4. Although a step response was chosen for convenience, in practice, change in i_y due to cloud movement is less severe. It was assumed that if the VCL performed satisfactorily when subjected to a step change in i_y then it should function satisfactorily under its normal operating conditions.

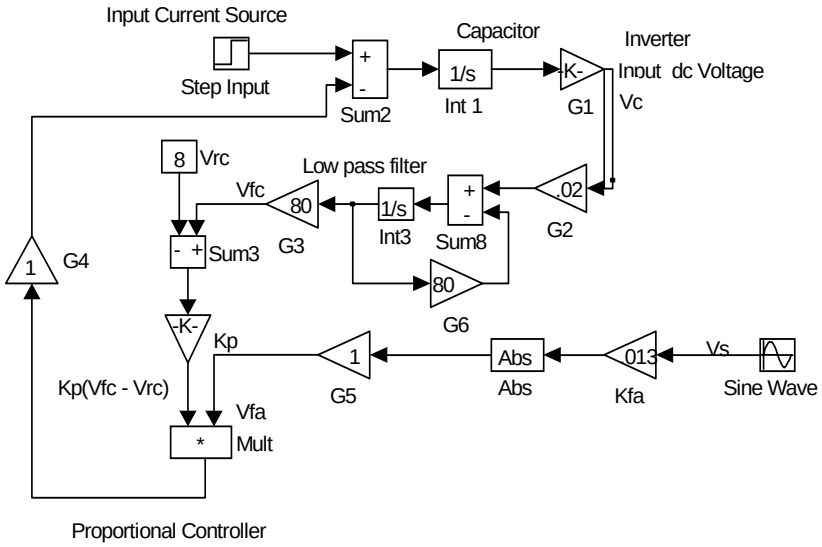


Figure 6.3: SIMULINK model of VCL with P-controller

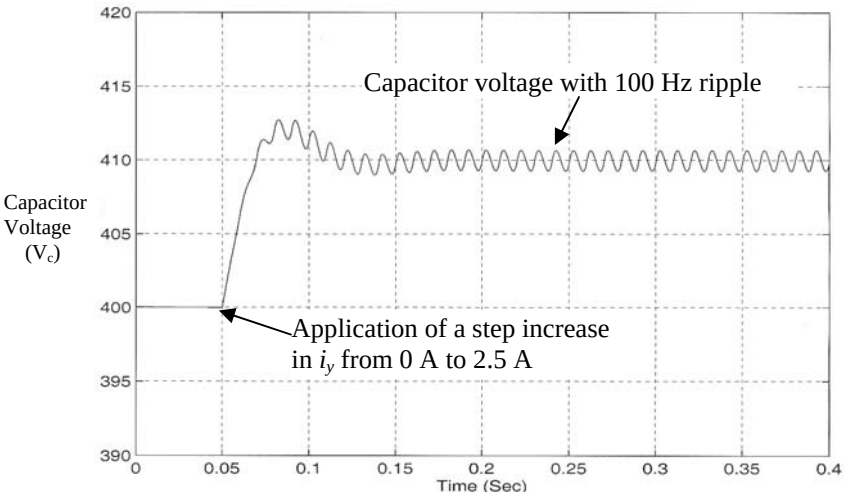


Figure 6.4: P-Controller response to a step change in DC input current i_y

The simulation results of the voltage loop using a P-controller show that:

- the steady state error was 10 V when the steady state value of i_y is 2.5 A
- the maximum overshoot in V_c is 2 V when the DC input current i_y is subjected to a step change of 2.5 A.

The steady state value of V_c, using the same VCL parameters in equation 6.7 is 410 V, and therefore agrees with the obtained results using SIMULINK.

6.4. Voltage Control Loop (PI-Controller)

Figure 6.5 shows the voltage control loop with a PI-controller and for convenience, the proportional gain K_p is kept the same as in the above case. Changing the voltage controller from P to PI makes it a third order system in which K_p controls the overshoot in V_c and K_{pi} controls the settling time and the zero error. It is not too difficult to realise that if the integral gain K_{pi} is too small then it will take a long time to reach zero steady error. On the other hand, if K_{pi} is too large (to improve settling time) then the system may become unstable.

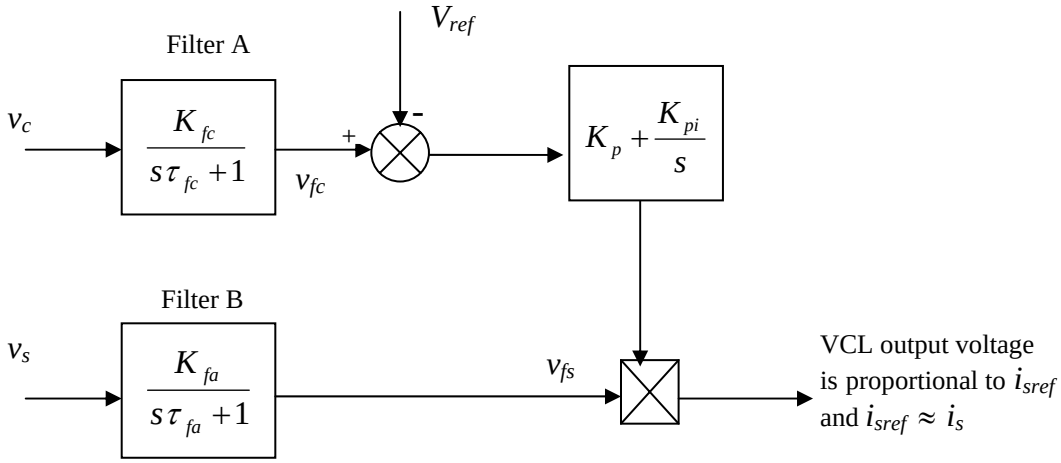


Figure: 6.5: Simplified VCL with PI-controller

With reference to Figure 6.1, the current through capacitor *C* is given by:

$$C\frac{dV_C}{dt} = I_y - i_s \tag{6.14}$$

Using Figure 6.5, the current fed to the grid system is: -

$$I_s = (K_p + K_{pi}/s)(\frac{K_{fc}V_c}{(1+s\tau_{fc})} - V_{ref})V_{fs} \tag{6.15}$$

Using equations 6.14 and 6.15 it can be shown that: -

$$V_c = \frac{\left(si_y + sk_p V_{ref} + K_{pi} V_{ref}\right)(1 + s\tau_{fc})}{s^2 C(1 + s\tau_{fc}) + sK_p K_{fc} + K_{pi} K_{fc}} \tag{6.16}$$

The steady state value of V_c can be obtained by applying the final value theorem to equation 6.17.

$$V_c = V_{ref} / K_{fc} \tag{6.17}$$

As expected there is no steady state error. The DC voltage V_c depends only on the reference voltage V_{ref} and the gain K_{fc} of the low pass filter A. To simulate the VCL using a PI-controller, K_{pi} needs to be chosen, such that the control loop remains stable. Therefore, the condition for stable operation of the VCL has to be determined.

Equation 6.18 was obtained by using linearised version of equation 6.1. All the variables in equation 6.18 represent small changes about the steady state values.

$$\frac{\Delta v_c}{V_c} = \frac{\Delta i_y s(1 + s\tau_{fc}) / \tau_{fc} C}{s^3 + s^2(1/\tau_{fc} - I_y / CV_c) + s / CV_c \tau_{fc}(KK_p - I_y) + KK_{pi} / CV_c \tau_{fc}} \tag{6.18}$$

Where $K = K_{fc} K_{fa} V_s^2$

In practice $1/\tau_{fc} >> I_y / CV_c$ and $KK_p >> I_y$. Therefore, equation 6.18 becomes

$$\frac{\Delta v_c}{V_c} = \frac{\Delta i_y s(1 + s\tau_{fc}) / \tau_{fc} C}{s^3 + s^2(1/\tau_{fc}) + sKK_p / CV_c \tau_{fc} + KK_{pi} / CV_c \tau_{fc}} \tag{6.19}$$

Applying Hurtwitz's stability criterion to equation 6.19 gives the stability condition for the voltage control loop using a PI-controller (equation 6.20).

$$K_p / K_{pi} > \tau_{fc} \tag{6.20}$$

To simulate the voltage loop using a PI-controller, the same values of K_p (4.45) and τ_{fc} (0.05s) were used, as used in the simulation exercise for the voltage loop using

the P-controller. A suitable value of K_{pi} (K_{pi} =10) was chosen using equation 6.20 and the above values for K_p and τ_{fc} such that the system remained stable. These parameters were used in the SIMULINK model of the VCL (with PI controller), shown in Figure 6.7, to determine its performance characteristics.

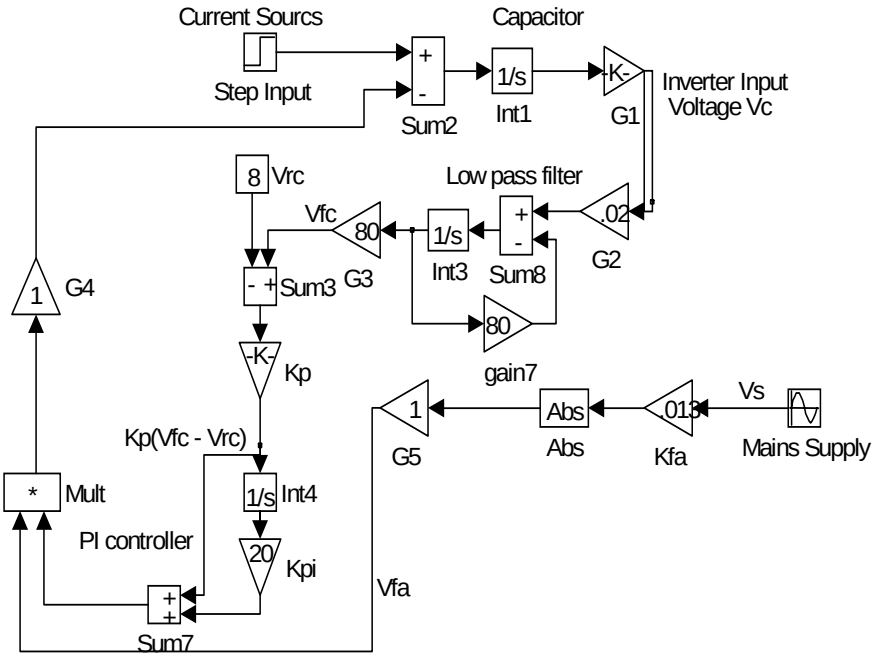


Figure 6.6: SIMULINK model of VCL with PI-Controller

The simulation results of the VCL (using PI controller) showing the inverter input DC voltage V_c when i_y is subjected to a step change of 2.5A, is presented in Figure 6.7. As expected, zero steady state error is achieved, and the maximum value of V_c was 412 V.

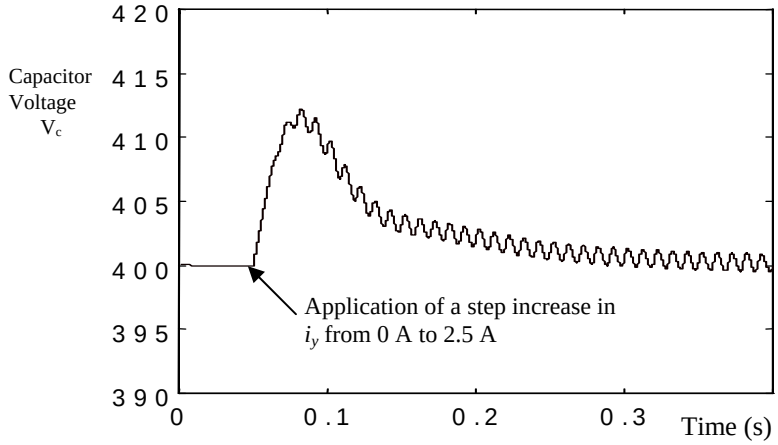


Figure 6.7: PI-Controller response to a step change in DC input current i_y

6.5. Response of the Voltage Controller to Mains Voltage Sags

The voltage loop simulations have been carried out so far with the assumption that the mains supply voltage V_s remains constant. In practice V_s may vary as much as 20% for a short duration when large loads are switched on. It was therefore important that the VCL using both types of controllers be subjected to such variations. To carry out this test a 20% step change in V_s was applied with I_s and V_c kept constant at 2.5A and 400V respectively (Figure 6.8). It was assumed that if the voltage loop performed satisfactorily when subjected to such extreme rate of change in V_s then under normal operating conditions its performance would be acceptable.

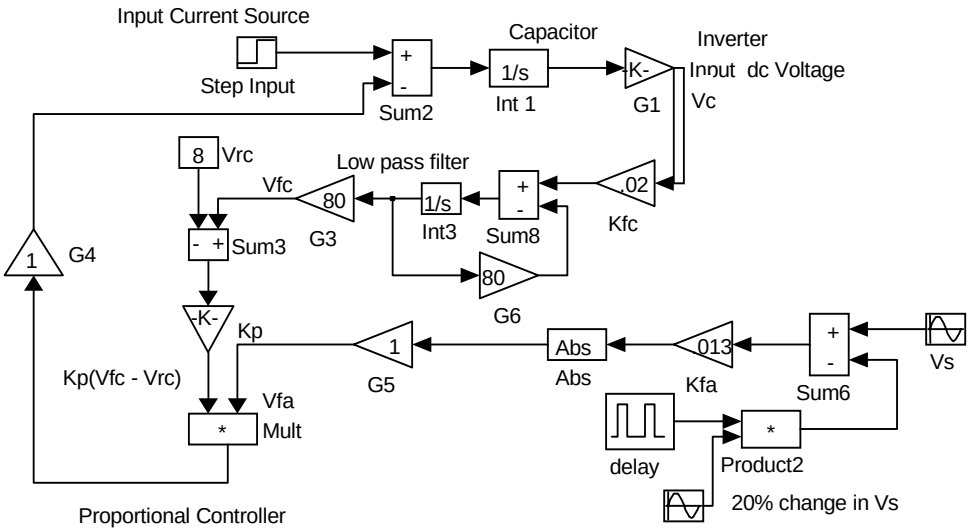
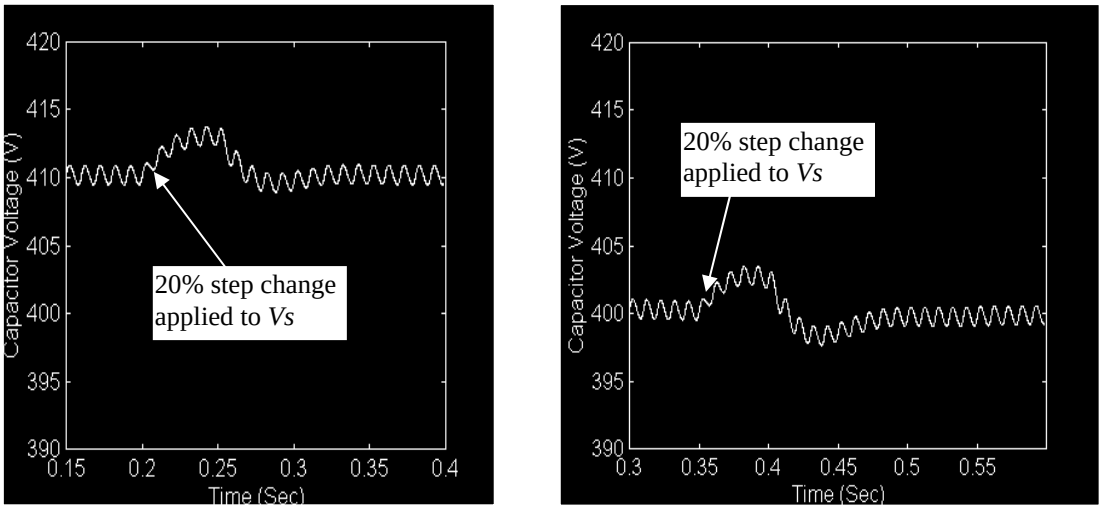


Figure 6.8: SIMULINK model of VCL to implement 20% change in supply voltage V_s

The result of the 20% step change in V_s is shown in Figure 6.9. To model a change in large inductive load that could cause such voltage variations for short durations, the duration of the step change was chosen to be 0.05 second. The voltage controller was able to adequately respond to this step change in V_s. As expected, when V_s is restored to its normal value, V_c returned to its original steady state value. This result demonstrates that the transient response of the VCL using both types of controllers, and the peak rise in V_c was as expected.



a) Voltage Loop using P-Controller b) Voltage Loop using PI-Controller

Figure 6.9: VCL response to 20% step change in V_s

6.6. Complete System Simulation

The final phase of the simulation process was to put together the complete inverter system using the same parameters for the voltage and current controllers as those used in sections 3.2 and 6.4. Figure 6.10 shows the SIMULINK model of the complete inverter system. Since one of the aims of this exercise was to establish if any interaction problems existed between the two controllers, the boost converter between the inverter and the panels was replaced by a perfect current source. The results of the inverter simulations are shown in Figures 6.11, 6.12 and 6.13. In Figure 6.11, the response of the voltage controller to a step change in I_y is the same as those obtained independently from the voltage controller (Figure 6.7).

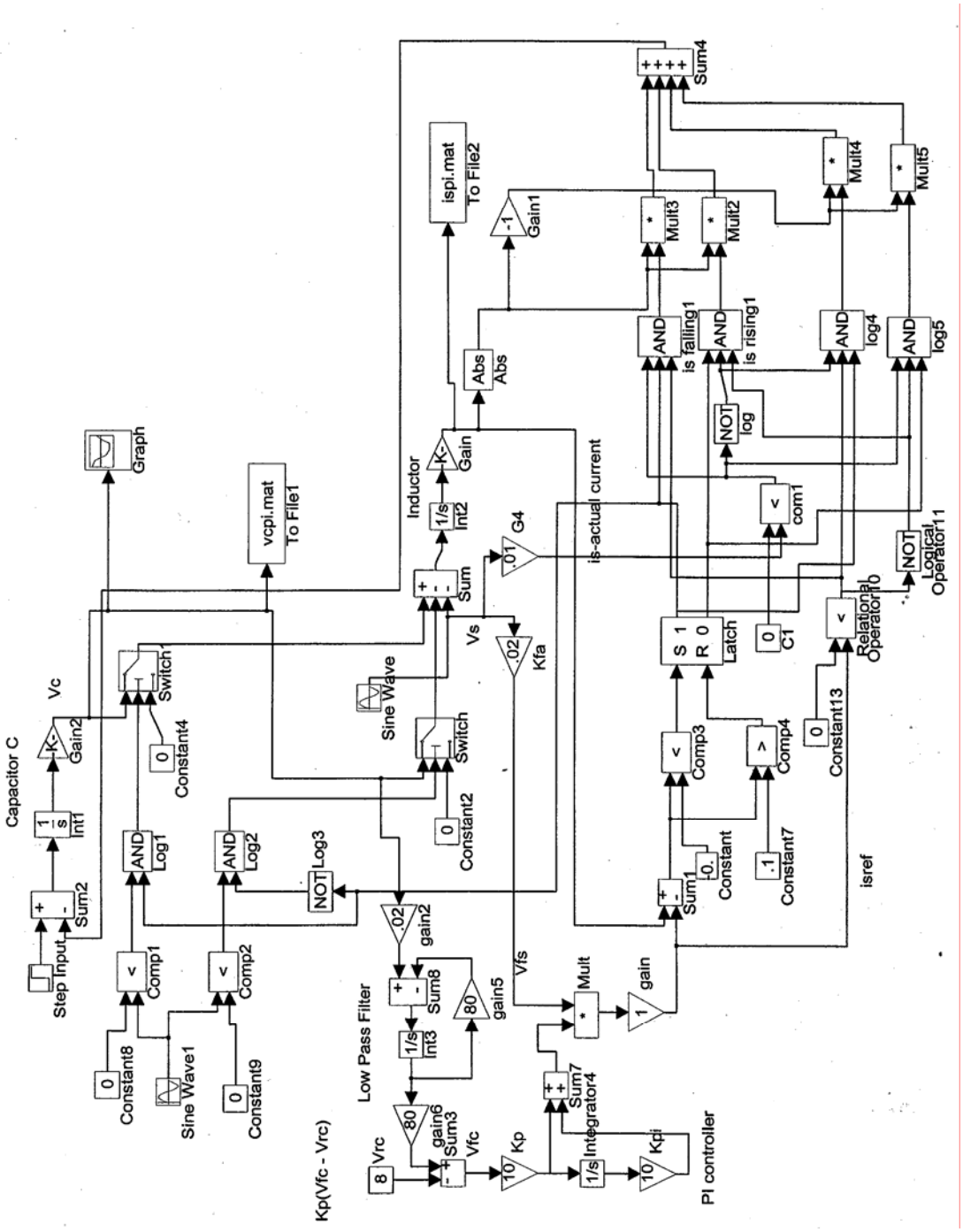
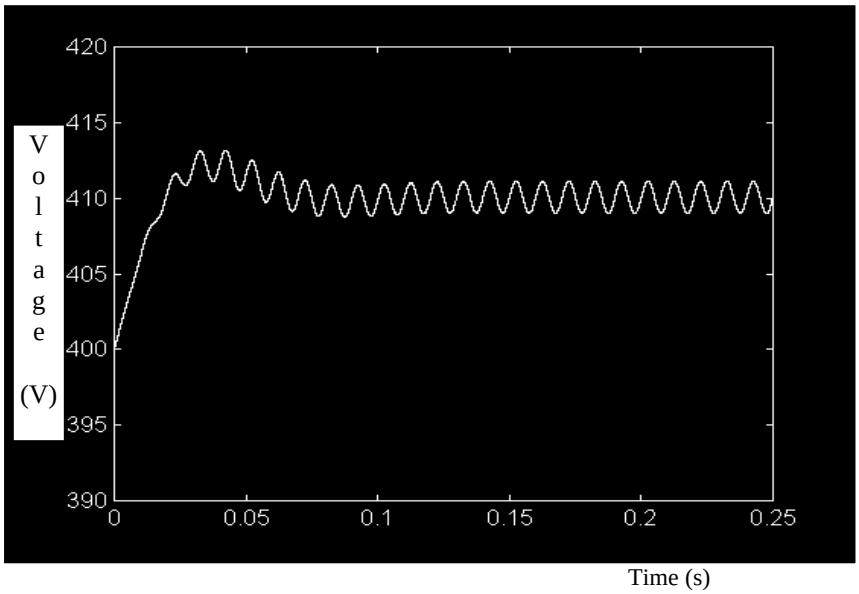
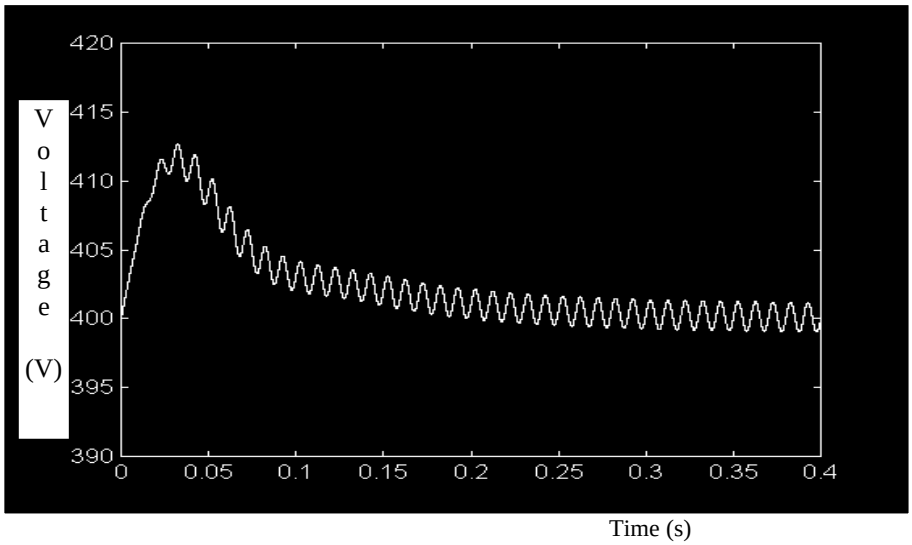


Figure 6.10: SIMULINK model of the Inverter VCL and CCL



a) Capacitor voltage using P-controller



b) Capacitor voltage using PI-controller

Figure 6.11: Capacitor voltage variations due to a step in i_y

When comparing the current spectrum of the complete system simulation results of the inverter shown in Figures 6.12 and 6.13, to that obtained for the current controller (Chapter 3, Figures 3.11 and 3.14) on its own, negligible difference in the magnitude of current harmonics was identified.

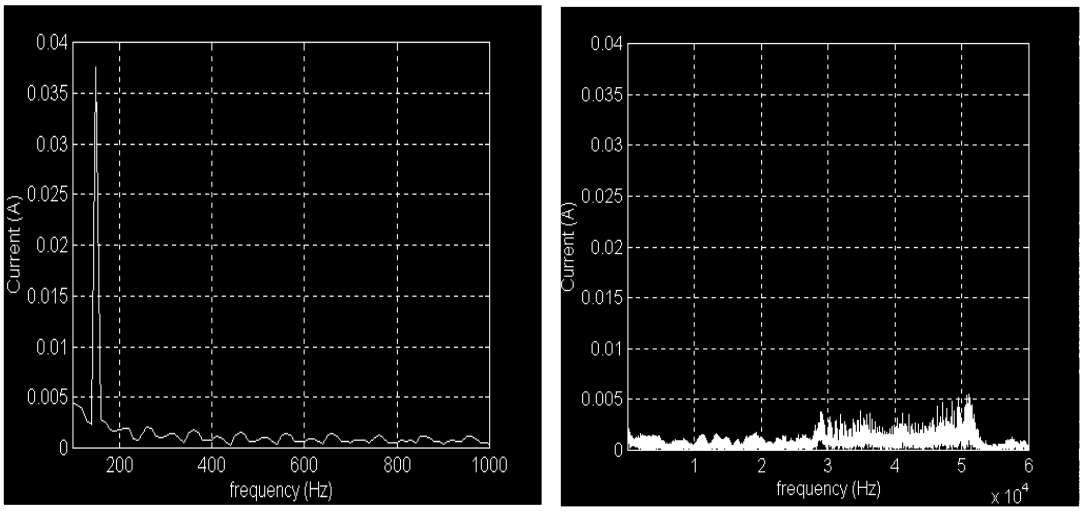


Figure 6.12: Frequency spectrum of I_s using P-controller

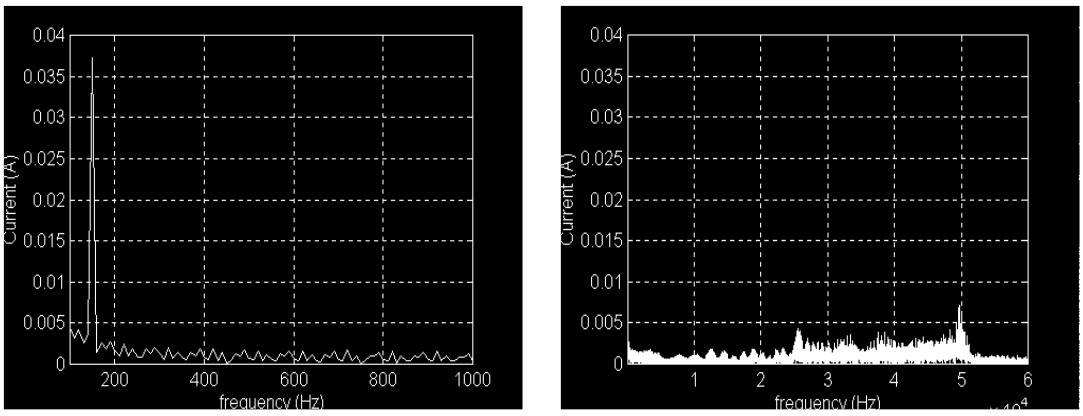


Figure 6.13: Frequency spectrum of I_s using PI-controller

For this example, these simulation results enable the following conclusions to be made: -

- There were no interactions of any significance between the VCL and current controllers that could lead to stability problems. Hence, the VCL and the CCL can be designed and tested independently.

- For the PV application being considered, at steady state, the integral control gain K_{pi} does not have any significant effect on the current harmonics present in I_s. Keeping K_p constant and changing only the value of K_{pi} confirmed this.

- The choice of K_p only influences the low frequency current harmonics that are present in I_s. The 3rd harmonic current I_{s3} increases from 0.6% to 1.5% when K_p is increased from 4.45 to 10. This is largely due to the decrease in V_c from 410 V to 403 V. A qualitative explanation to show the relationship between K_p and I_{s3} due to the 100 Hz ripple in V_c will be developed in section 6.7.

- Apart from the magnitude of I_{s3}, K_p also determines the steady state value of V_c. If in equation 6.7 K_p is varied while all other variables are kept the same, as in section 6.3, the results obtained are shown in Figure 6.14.

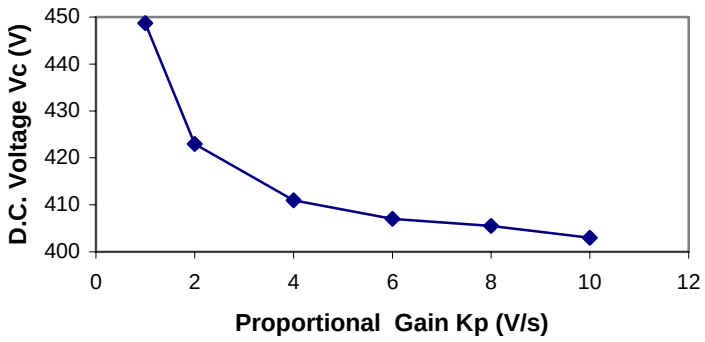


Figure 6.14: Relationship between K_p and V_c

An advantage of using the P-controller is that it does allow the designer the flexibility to choose lower values of V_c for light loads and higher values of V_c as I_s increases. For example, if I_y is increased from 0 to 2.5A (which corresponds to an increase in I_s from 0A to 4.2A), the steady state value of V_c increases from 400V to 410V. The advantages of this are as follows: -

- It is easier to maintain the value of V_c above $\hat{V}_S$ and avoid unwanted distortion of I_s

- the steady state error helps keep the switching frequencies within a tighter band and therefore this helps in the design of the SFF.
- the switching loss is marginally reduced at light loads

The maximum power from a PV generator (solar panels in fixed position) occurs only for a short while, around midday and for most of the day I_s is below its rated value. Hence, for inverters used for utility connected PV systems, a P-controller with a small steady error in V_c was acceptable because of the advantages identified earlier.

The simulation results of the VCL using the P-controller suggested that it was suitable for use in utility connected PV inverters. Since the magnitude of harmonic currents using the P-controller are well below those specified by the Australian Standards [4], it was chosen in preference to the PI-controller for this project.

6.7. Estimation of 3rd Harmonic

The aim of this project is to improve the efficiency of an inverter system without compromising the quality of the current I_s. It is therefore important to be able to minimise the level of the third harmonic (I_{s3}) in I_s contributed by the voltage control loop.

The second harmonic current I_{s2} (equation 6.21) was derived using the output of the inverter-bridge $\frac{2\hat{I}_s}{\pi}$ and the generalised ripple voltage equation 2.81, given on page 93 of the text by Bird and King [65].

$$\hat{I}_{s2} = \frac{4\hat{I}_s}{3\pi} \tag{6.21}$$

The capacitor voltage V_c has a second harmonic component (V_{c2}) and is determined using equation 6.22. When V_{c2} is multiplied by V_{fs} (Figure 6.2), the result is the generation of a third harmonic component which is present in I_{sref}.

$$\hat{V}_{c2} = \frac{\hat{I}_{s2}}{2\omega C} \tag{6.22}$$

Since the inverter is to operate at unity power factor, equations 6.2, 6.3, 6.21 and 6.22, can be used to developed equation 6.23 to estimate third harmonic current $I_{s3.}$

$$I_{s3} = \frac{\sqrt{2}V_s K_{fc} K_{fa} K_p I_s}{3\pi\omega C\sqrt{4\omega^2 \tau_{f_c}^2 + 1}} \tag{6.23}$$

The supply authorities set the value of V_s and the gain product $K_pK_{fc}K_{fa}$ is chosen to achieve a given settling time of V_c due to a step change in i_y. As expected, the magnitude of I_{s3} can only be controlled by the capacitor C and the time constant τ_{fc} of filter A. Although a step change in i_y was used to determine the transient response of the control system, in practice, the change due to cloud movement, is far more gradual [2].

Equation 6.23 also confirms that attempts to reduce the steady state error in V_c by increasing K_p (Figure 6.14), will have the undesirable effect of increasing the level of third harmonics in I_s. It will however, be shown in the next section that if the values of C and τ_{fc} are carefully chosen, the magnitude of I_{s3} can be kept within the specified legal limits [4]. Also, the values of third harmonics generated by the VCL are very much less than those attributed to the CCL (as analysed in Chapter 3).

6.8. Design of Voltage Control Loop

The current supplied to the grid needs to be sinusoidal at nearly unity power factor. The harmonic current injected into the utility system, and the total harmonic distortion (THD), have to be acceptable to the supply authorities.

The important conditions therefore, for the system shown in Figure 6.1 that need to be addressed are: -

- Maximum allowable ripple in i_p
- Maximum and minimum allowable values for v_c
- Maximum allowable harmonic distortion in i_s
- Specified transient response time and percentage overshoot for v_c

With the above four specifications in mind, it was decided that the inverter control system should meet the following performance criteria: -

- Steady state increase in V_C (400 V) should not be more than 10 V as I_y increases from 0 to its rated value of 2.5 A or when a sag of up to 20% in V_s occurs;

- Settling time for v_c as a result of a step change in i_y, or when a 20% sag in v_s occurs, should not be longer than 0.1s ;

- Overshoot as a result of a 2.5 A step change in i_y should not exceed 20%, that is v_c should not exceed 412 V or 420V when there was a 20% sag in v_s at rated current;

- The second harmonic component in v_c must not exceed 5 V peak

- The third harmonic component in i_s due the second harmonic component in v_c must not exceed 1% of I_s.

To design the voltage loop using equations 6.7, 6.13 and 6.23, it is far more convenient to express these equations in term of the design specifications. For practical reasons, the rise in V_c as I_y increases (equation 6.7) must be kept small. The per unit rise in V_c at rated power P_r can therefore be given by:

$$\frac{\text{rise in } V_c}{V_{cr}} = \mathrm{E_{ss}} = \frac{P_r}{K_p K_{fc} K_{fa} V_{cr} V_{sr}^2} \tag{6.24}$$

$$\therefore K_p K_{fc} K_{fa} = P_r \big/ E_{ss} V_{cr} V_{sr}^2 \tag{6.25}$$

where V_{cr} is the rated DC supply voltage and V_{sr} is the ratedAC supply voltage

As mentioned earlier, in practice the term KI_y in equation 6.13 is smaller than 1. Also, by design the term $K_p K_c K_{fa} V_{sr}^2$ will normally be very much larger than I_y. Equation 6.26 is a simplified version of equation 6.13, which may therefore be regarded as applicable for any load level.

$$\frac{\Delta V_C}{V_C}\left(\frac{P_r}{E_{ss} V_{cr}}\right) \approx \left[1 + \frac{P_r \tau_{fc}}{E_{ss} V_{cr}^2 C}\left\{\frac{(1-a)e^{-at/\tau_{fc}}}{a(a-b)} + \frac{(1-b)e^{-bt/\tau_{fc}}}{b(b-a)}\right\}\right] \tag{6.26}$$

$$\text{where a, b} \approx \frac{1}{2} \pm \left[\frac{1}{4} - \frac{\tau_{fc} P_r}{E_{ss} V_{cr}^2 C}\right]^{0.5}$$

Equation 6.27 is the normalised form of equation (6.23).

$$\frac{3\pi}{\sqrt{2}} \cdot \frac{I_{s3}}{I_{pr}} \cdot \frac{1}{\sqrt{1+4I_{pr}}} \cdot \frac{V_{sr}}{V_{cr}} = \left(\frac{\tau_{fc} P_r}{E_{ss} V_{cr}^2 C}\right) \cdot \frac{1}{\omega \tau_{fc} \sqrt{4\omega^2 \tau_{fc}^2 + 1}} \tag{6.27}$$

Since no isolation transformer was used, then there was no freedom on the choice of V_s. Design of the inner loop would dictate the choice V_{cr}/V_{sr}, which was normally in the 1.6-1.8 range. Since the voltage controller is to be designed for a 1 kW unipolar switched inverter system, the value of the rated power of P_r is known. Hence, the design of the VCL involves determination of values for the product $K_p K_c K_{fa}$, capacitance C and the time constant τ_{fc}. Controller specifications include the following: -

- full load steady state error (E_{ss})
- percentage overshoot of ΔV_c
- settling time of ΔV_c
- third harmonic in i_s.

To proceed with the simulations, the values for the gain product $K_{fa}K_pK_{fc}$, had to be chosen so that the steady state error (E_{ss}) in V_c is limited to 2.5% (10V) when i_y was a step input of 2.5 A. Using equation 6.23 and 0.02 as the values of K_{fa} and K_{fc} (to prevent saturation of the amplifiers during implementation), the gain K_p was found to be 4.34. The values chosen for V_c and V_s were 400 V and 240 V respectively.

To find suitable values of C and τ_{fc} equation 6.24 was first used to produce Table 6.1. This table illustrates that for the very small cost of a low pass filter, significant reduction in the 3rd harmonic can be achieved. The use of this filter also gives the designer the ability to control the settling time of v_c due to changes in I_y. Since a 3.9 mF capacitor was readily available, it was used to obtain the value of τ_{fc} such that the magnitude of the 3rd harmonic current I_{s3} was less than 1% or 0.06A (maximum limit specified by AS4777.2, 2005). A time constant of 0.05s was chosen for τ_{fc}. Using these values for C and τ_{fc}, the calculated value of 3rd harmonic current I_{s3} was about 0.012 A.

	0	0.005	0.01	0.015	0.02	0.025	0.03	0.035	0.04	0.05	τ_{fc} (s)
C(F)											
0.001	1.5112	0.4584	0.2375	0.1594	0.1199	0.096	0.0801	0.0686	0.0601	0.0481	Is_3 (A)
0.0015	1.0075	0.3056	0.1584	0.1063	0.0799	0.064	0.0534	0.0458	0.0401	0.0321	Is_3 (A)
0.002	0.7556	0.2292	0.1188	0.0797	0.0599	0.048	0.040	0.0343	0.030	0.0240	Is_3 (A)
0.0025	0.6045	0.1833	0.095	0.0638	0.048	0.0384	0.032	0.0275	0.024	0.0192	Is_3 (A)
0.003	0.5037	0.1528	0.0792	0.0531	0.040	0.032	0.0267	0.0229	0.020	0.0160	Is_3 (A)
0.0035	0.4318	0.131	0.0679	0.0456	0.0343	0.0274	0.0229	0.0196	0.0172	0.0137	Is_3 (A)
0.004	0.3778	0.1146	0.0594	0.0399	0.030	0.024	0.020	0.0172	0.015	0.0120	Is_3 (A)

Table 6.1: Simulation results of I_{s3} as a function of C and τ_{fc}.

Using the above values for C and τ_{fc}, the transient response of the voltage loop was obtained from equation 6.13. As expected the maximum value and the steady state value of v_c (Figure 6.15) were 412 V and 410 V respectively. The settling time for v_c was 0.06 seconds. This theoretical result met the design specifications and was the first step towards validating the assumptions made to simplify the design equations.

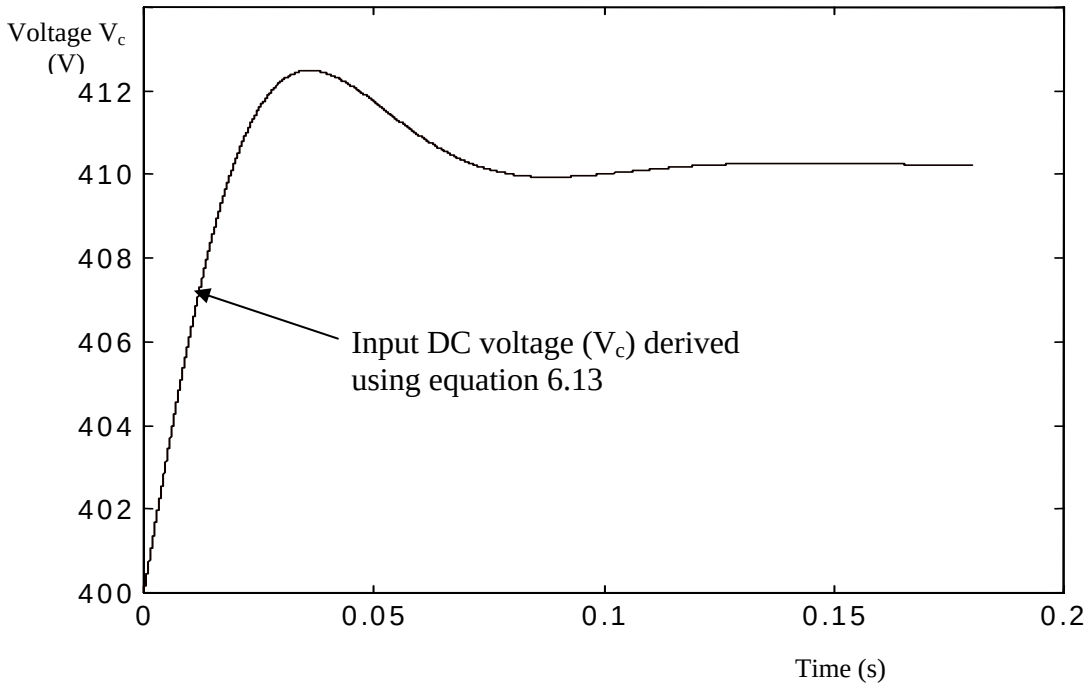


Figure 6.15: Theoretical transient response of the Voltage Control Loop due to a step change in i_y.

The next step was to use the SIMULINK model of the complete inverter system described in Figure 6.10 to validate the design procedure. The result of a step change in i_y occurring 0.3 seconds after the inverter was switched is shown in Figure 6.16. The steady state, transient response, the settling time and the maximum value of v_c results all agree with the design specification.

Finally a 20% step change in V_s was applied to the complete inverter system and the results shown in Figure 6.17 met the required specifications. Experimental verification of the design procedure of the VCL is presented in next chapter.

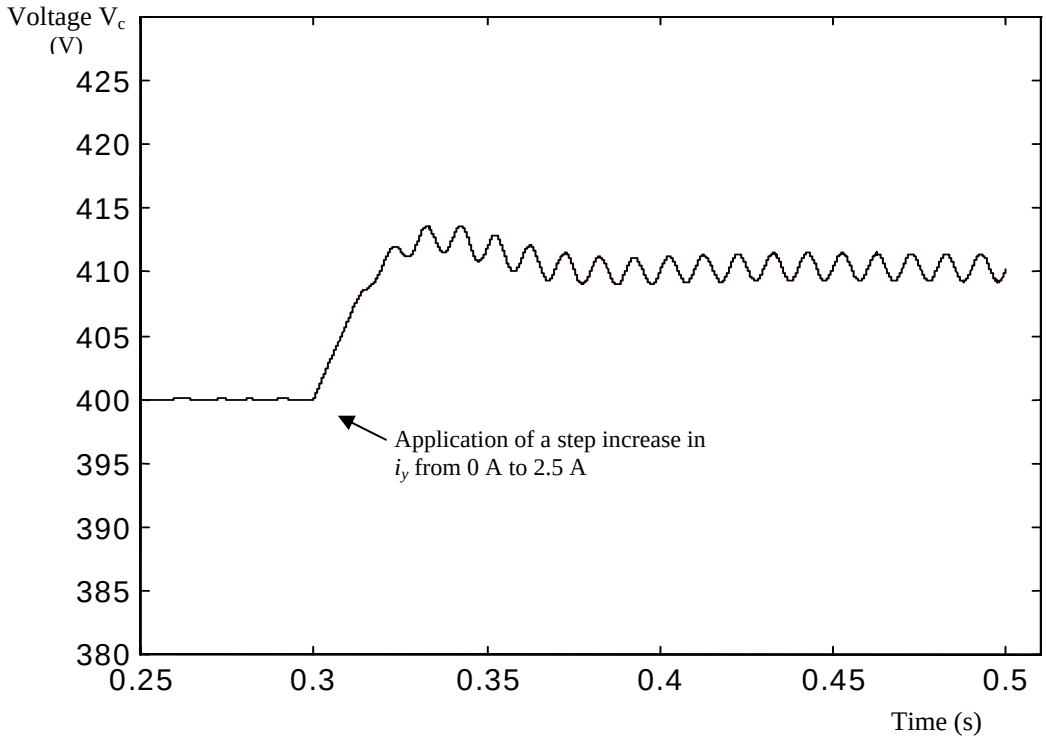


Figure 6.16: Simulated transient response of the inverter system due to a step change in i_y

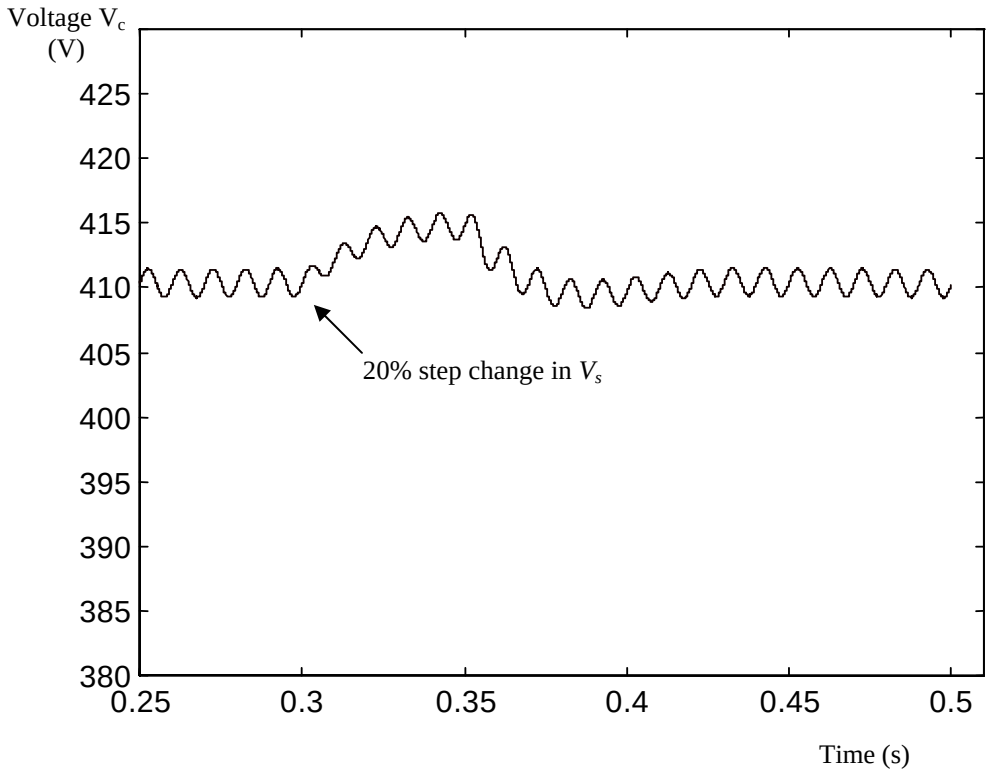


Figure 6.17: Simulated voltage controller response to 20% step change in V_s

6.9. Conclusions

The simplified models of the voltage control loop using both the P-controller and the PI-controller have been realised.

The models have been used to establish that: -

- there is no significant difference in the level of harmonics between the two types of controllers to prevent the P-controller being used in the unipolar switched inverter in this project.

- the steady state characteristics and the transient response of the VCL using the P-controller met the desired specifications

- the capacitor *C*, the time constant of the low pass filter τ_{fc} and the proportional gain K_p can be chosen from Table 6.1, such that, the inverter DC input voltage regulation is acceptable and the level of the third harmonic current I_{s3} was maintained below the legal limits.

- there were no interactions between the voltage and the current controllers that prevented the two controllers from being designed separately.

Finally, work carried out in this chapter validates the use of SIMULINK models (section 6.3) and a set of reasonable VCL parameters to determine the performance of the VCL.

CHAPTER 7

VOLTAGE LOOP: DESIGN AND TESTING

7.1. Introduction

Circuits designed to implement the VCL developed in Chapter 6, and experimental results to verify its performance are presented in this chapter. The performance results for the VCL with the current controller and the switching frequency filter are also outlined in this chapter.

Since a transformerless unipolar switched inverter system is being considered, it is necessary to establish if the DC offset current being injected into the grid system is less than 5 mA or 0.5% of the rated output (whichever is greater) [4]. Despite the exhaustive literature review carried out in Chapter 2, published information related to the main contributors or typical levels of DC offset current present in the output of PV inverter systems was not available. Therefore, in this chapter, the main sources of DC offset currents had to be identified and the magnitudes of these currents recorded.

It has been confirmed in Chapter 6 that a steady state error in V_c will exist as a result of using the P type controller. In this chapter attempts are made to measure the small increase in switching losses arising from an increase in V_c.

7.2 Voltage Loop Circuit Design

As previously mentioned, the purpose of the VCL was to provide the current controller with the sinusoidal current i_{sref} of correct magnitude, phase and frequency such that the input DC voltage V_c remains constant at a predetermined value, in this case 400 V. A simplified schematic circuit diagram and the corresponding test circuit of the voltage

controller are Figures 7.1 and 7.2. The AC voltage v_s from the output of the voltage transformer VT is buffered by the unity gain voltage follower TC13 and passes through zero phase-shift filters TC14 and TC15 (Filter B). These filters remove harmonics present in the supply voltage as shown in Figure 7.3. Total harmonic distortion (THD) of the supply voltage, available for this project, was about 2%. The percentage of lower order harmonics present in the supply voltage is given in Figure B5 (Appendix B).

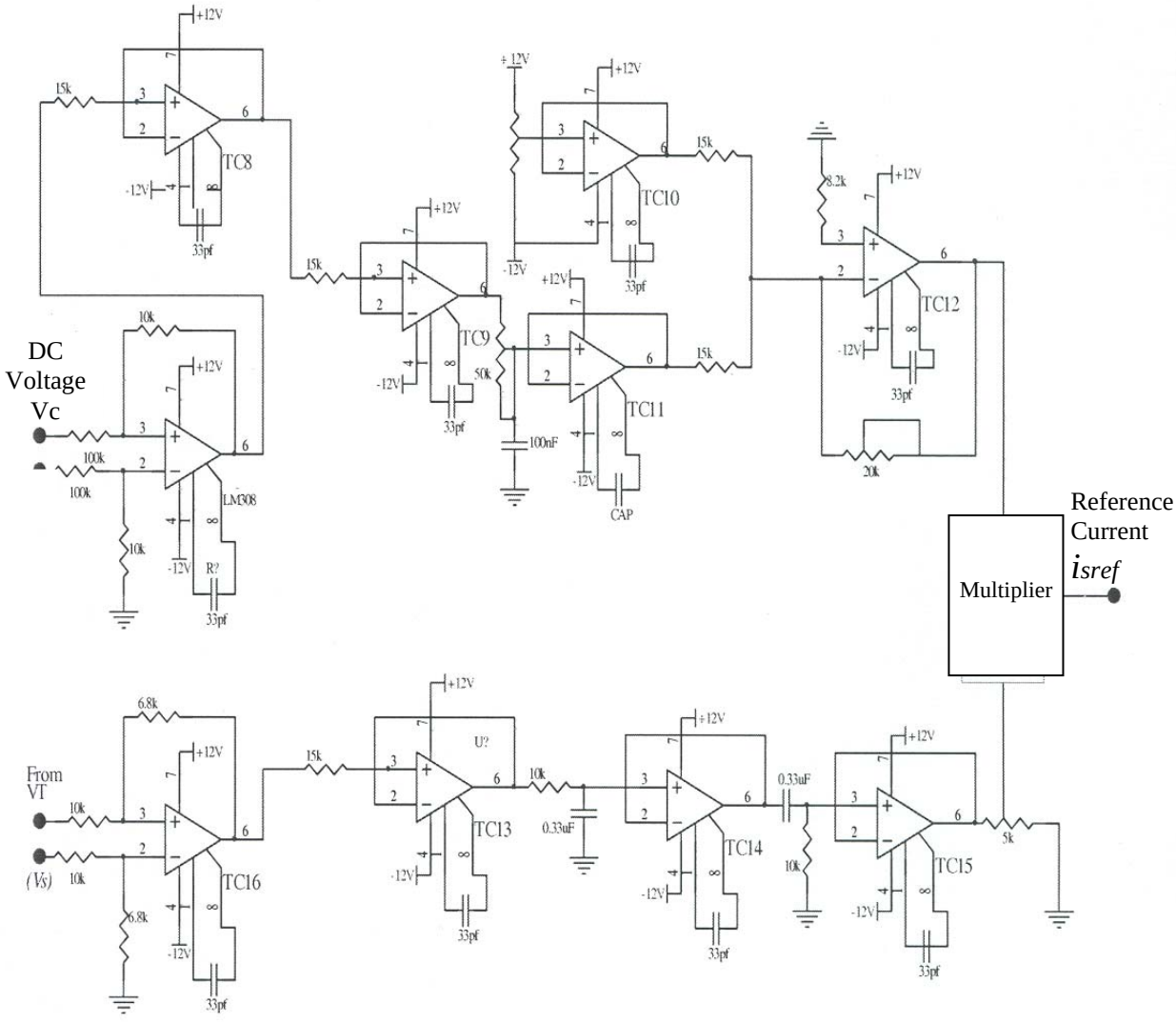


Figure 7.1: Schematic diagram of voltage control loop

The total voltage gain from the primary side of VT to the input of the multiplier is k_{fa}. The magnitude of this attenuated voltage is $k_{fa}.v_s$ and the actual value of k_{fa} is obtained from the design procedure in Chapter 6.

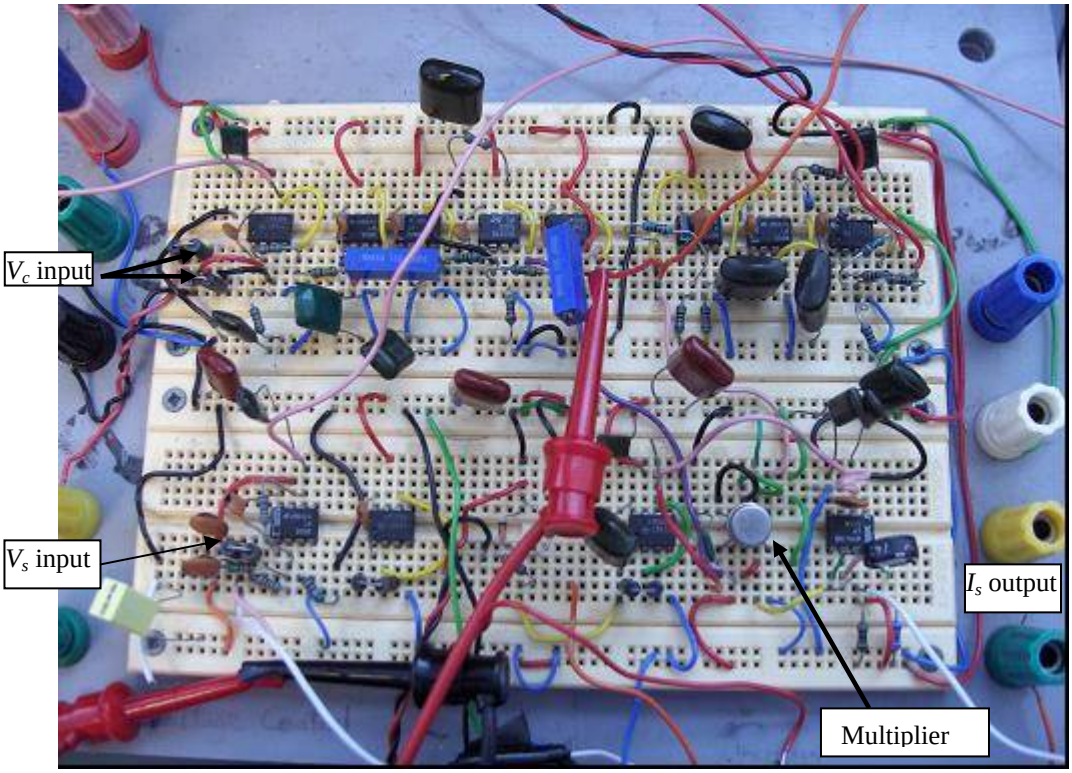


Figure 7.2: Voltage control loop test circuit

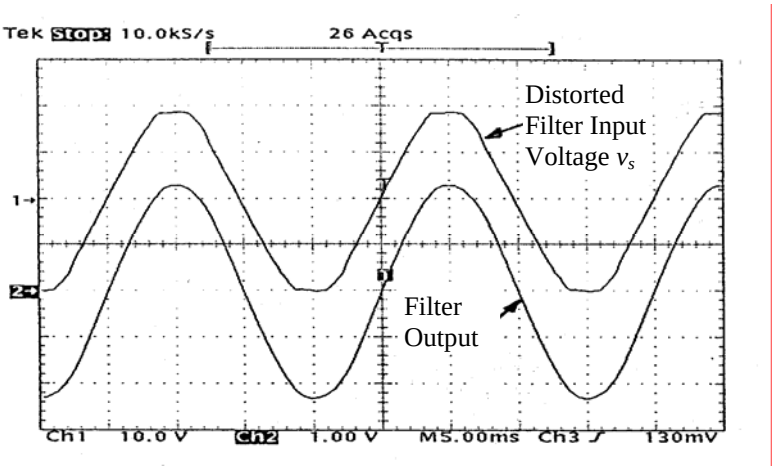


Figure 7.3: Zero phase-shift filter output

The DC voltage V_c is also attenuated and buffered by the voltage follower TC8. The output of TC8 passes through a low pass filter (filter A) whose function is to reduce the 100 Hz ripple present in V_c. The product of k_{fc} and V_c becomes one of the inputs at the summing-junction of TC12, where k_{fc} is the gain of the circuit from the DC input voltage to the input of TC12. This gain is taken as 0.02 and is again obtained from the design procedure in Chapter 6. The second input at this summing-junction is the DC reference voltage V_{ref}. This value is proportional to the no-load steady state value of V_c which in this case was set to 8 V ($V_{ref} = k_{fc}.V_c$). The difference between V_{fc} and V_{ref} is the error in V_c and is amplified using TC12. The gain of this amplifier is k_p and the value of k_p obtained from the design procedure is 2.6.

The output of the multiplier i_{sref} is the inverter reference current,

where $$i_{sref} = (V_{fc} - V_{ref}) k_p V_{fs.} \quad (8.1)$$

Current i_{sref} is a sinusoidal wave that is in phase with the supply V_s and has a magnitude proportional to the error voltage (equation 8.1). Hence, the inverter output will always be automatically synchronised with the grid supply. The inverter output

current i_s is forced to stay within a small tolerance band around i_{sref} by the current controller as described in Chapter 3.

7.3. Verification of Voltage loop Design

For convenience the test circuit shown in Figure 7.4 was initially used to obtain the steady state response of the VCL. To ensure better control of the input DC voltage, a DC source (0 to 600V) in series with resistor R_1 was used to model the output characteristics of the solar panels. As the DC source voltage was varied above or below the value preset by the reference voltage V_{cref}, the current I_s will automatically be adjusted by the voltage controller such that the capacitor voltage V_c remains constant.

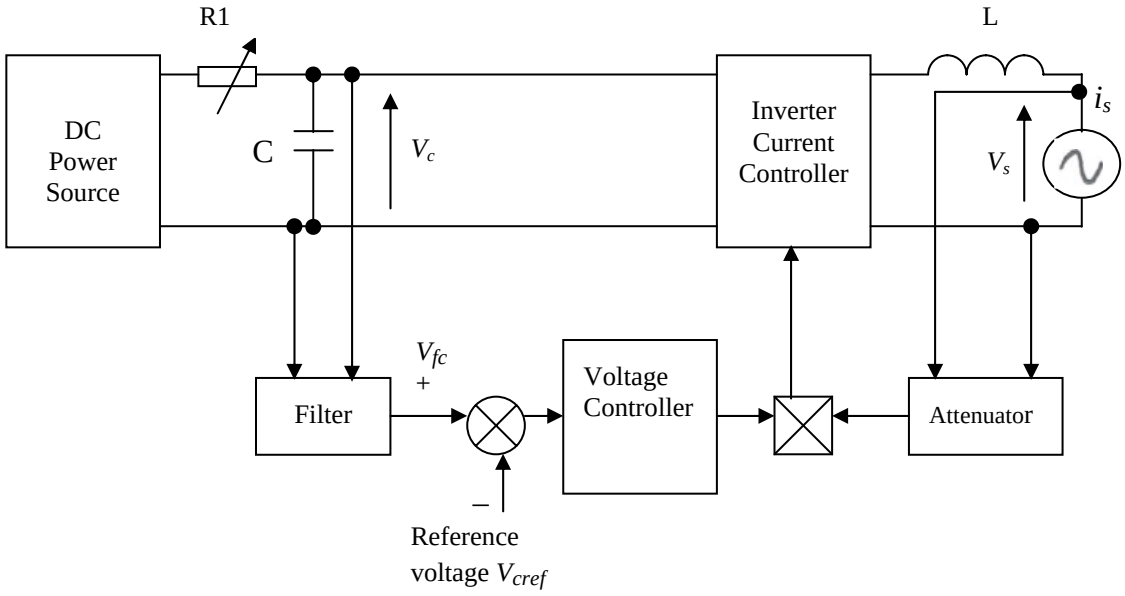


Figure 7.4 Voltage controller test circuit

The steady state error in the DC voltage V_c across the capacitor as the current I_s supplied by the inverter system was increased from 0 to 4 A is shown in Figure 7.5. These results have been obtained using the voltage control circuit shown in Figure 7.1 and the loop parameters determined in Chapter 6. The maximum difference between the theoretical prediction and experimental results, for the 1 kW inverter system being considered, was about 4.0%. This small difference between the theoretical and experimental value of V_c was considered acceptable. These results validated the VCL

design procedure developed in Chapter 6. As stated earlier, the advantage of this error in V_c is that it will assist in maintaining the current harmonics in the inverter output at an acceptable level as the current I_s reaches its rated value.

The disadvantage of this 4% error in V_c, is a small increase in switching power losses. Attempts to measure this small (in the tens of mW range) increase in switching loss, in a noisy environment with the instrumentation available proved very difficult.

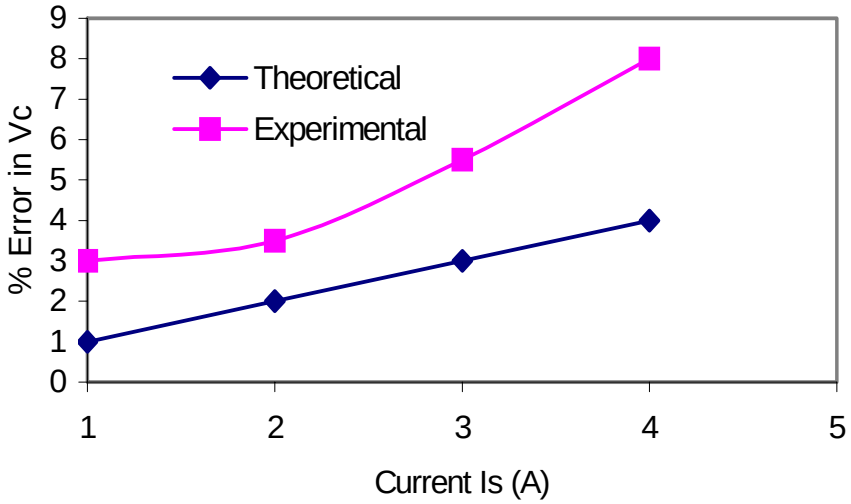


Figure 7.5 Steady state error in V_c

A benefit of this exercise was that it justified the use of a fixed reference voltage V_{ref} rather than a variable reference voltage to maintain the ratio V_s/ V_c constant. Compensating variations in mains supply voltage V_s by varying V_c, may yield a very small saving in switching losses. However, the cost of the control circuits and the power losses of these circuits required to keep the ratio V_s/ V_c constant, may not make the use of a variable DC reference a viable option.

The transient behaviour of the voltage control loop, which would normally be caused by cloud movement, was very difficult to measure. Simple tests (using the circuit arrangement shown in Figure 7.4) such as applying a sudden increase or decrease of about 20% in the DC power supply voltage to simulate cloud movement and

monitoring the DC voltage V_c and I_s was considered adequate to demonstrate the dynamic response of the voltage loop. The time taken for the voltage controller to adjust the current I_s, and for v_c to reach a steady state value, were difficult to measure accurately but both were less than 0.5 seconds. However, the importance of this test was that it demonstrated that there was no stability problem associated with the VCL.

7.4. Inverter System Test Results.

Tests results carried out using the inverter VCL, the CCL and the switching frequency filter to supply power to the grid are shown in Figure 7.6. The results presented in Figure 7.6 show the inverter system injecting current into the grid supply. The inverter input power was supplied from a 1 kW PV system shown in Appendix E.

To determine the increase in the level of 3rd harmonics (due to the VCL) the inverter system was tested with and without the VCL. It was difficult to measure any increase in the 3rd harmonics because there was no noticeable increase due to the VCL. The FFT of the filtered current showed that the switching frequency harmonics were attenuated and that no unwanted switching occurred at the zero crossing.

The only remaining issue that may prevent connection of the proposed transformerless inverter system to the grid network was the magnitude of the DC offset current component in I_s.

While techniques to reduce lower order harmonics for multiple inverter systems by Armstrong et al. [66] and the reduction of THD for grid connected inverters by Abeyasekera et al [67], was successfully achieved, the presence of DC offset current was ignored by them. Hence, this issue will be discussed in the next subsection.

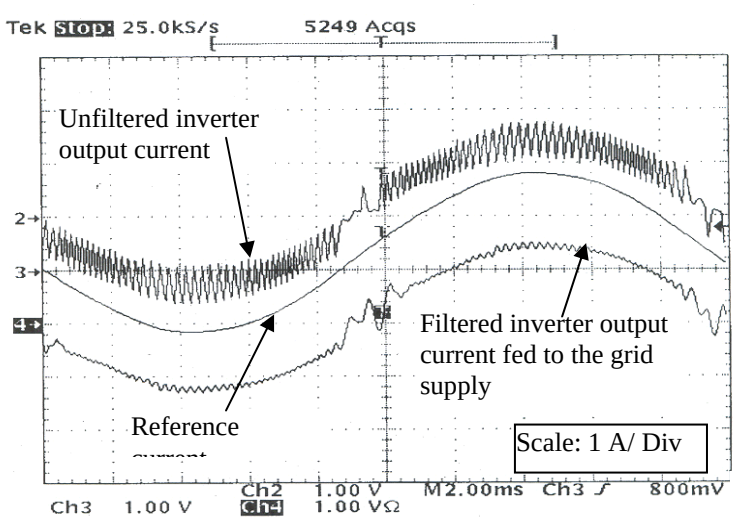


Figure 7.6 Inverter Test Results.

7.5. Sources and Magnitude of DC Offset Current

The level of DC offset current measured at the inverter output was found to vary between 12 mA to 34 mA when the current I_s was varied from 0A to 2A. This is unacceptable, as 34 mA is well above the maximum level of 21 mA specified by the Australian standard [4]. To achieve the aims of this project, the problems of illegal magnitudes of DC offset current being injected into the grid system had to be solved.

To correct this situation, the main sources that contributed towards the presence of DC offset current in the inverter output needed to be identified. Measurements carried out revealed that the contribution of DC offset current by the VCL (DC component in reference V_{ref}) and that due to the inverter bridge (not being symmetrical), was found to be negligible.

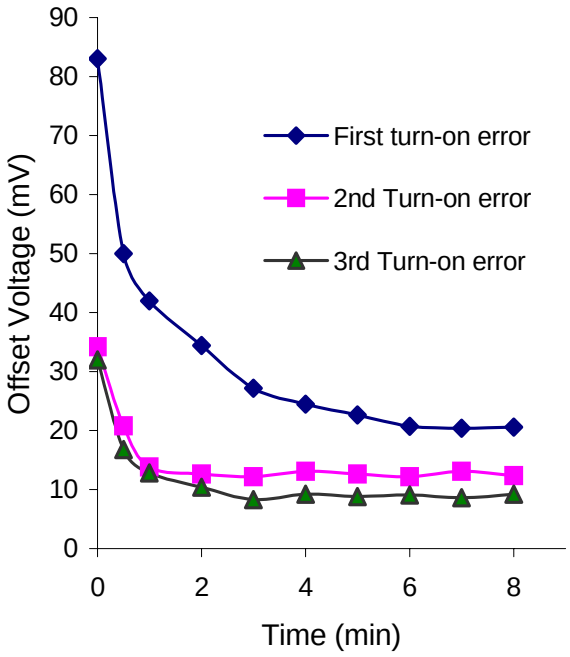


Figure 7.7 Hall Effect Current Sensor Output

Experimental results confirmed that the Hall Effect current sensor was the dominant contributor of the DC offset current present in the inverter output. Figure 7.7 shows the DC offset error of the Hall Effect sensor when V_c, V_s and I_s were all equal to zero. When the DC power supply to the control circuits and the Hall Effect sensor was first turned on, the initial DC offset current recorded was 83 mV. Since the current sensor was calibrated to give an output of 1 V when I_s was 1 A, this 83 mV represents an error of 83 mA when the actual value of I_s was zero. This procedure was then repeated several times. The results from the first, second and third attempts were recorded (Figure 7.7). These results were obtained at a room temperature of 18^0 C.

It was necessary to establish if correcting the DC offset current error introduced by this relatively low cost Hall Effect current sensor was a viable option. To carry out this exercise, known values of DC voltages were added to the reference signal and the actual value of DC offset current component present in the current sensor output was recorded (Figure 7.8). When 27 mA of DC current was added to the reference current, the Hall Effect sensor output indicated 0.2 mA and when 0 mA DC offset current was applied to the reference current, the sensor output was 26.8 mA.

Although Armstrong et al [68] developed an auto-calibrating DC link current sensing technique capable of limiting the DC offset current, these experimental results have established that correcting the DC offset error introduced by the current sensor was not a suitable option. It could lead to unacceptable magnitudes of DC offset current being injected into the grid system. Therefore, the best option was to remove the DC offset current from the inverter AC output current. In this way irrespective of its source, the actual DC offset component present at the inverter output is being measured, separated and then removed from the AC current.

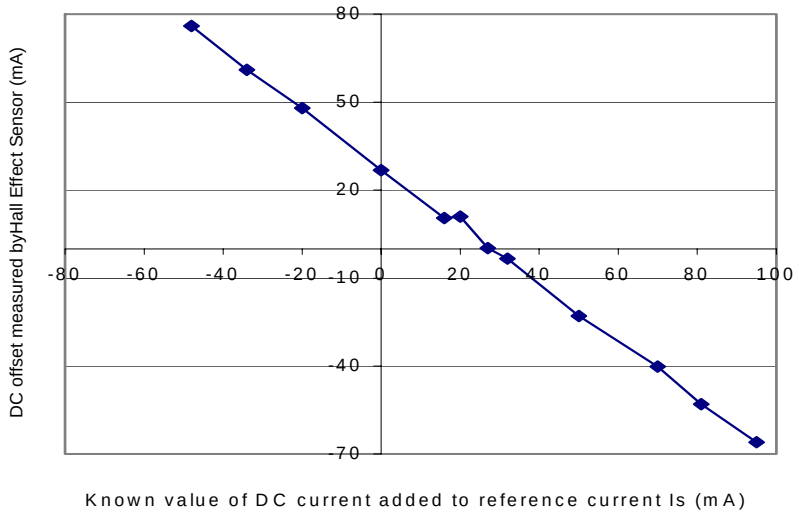


Figure 7.8 DC offset current from Hall Effect Current Sensor

Since one of the aims of this project is to avoid the use of 50 Hz power transformers, a DC offset current controller had to be designed to perform the DC current removal function, efficiently and cost effectively. Failure to do so would nullify the benefits of

avoiding the use of transformers. The development of a new DC offset current loop that maintains the level of DC current injected into the grid network within the levels stipulated by Australian Standard will be dealt with in the next chapter.

7.6. Conclusions

The voltage loop with its proportional controller operated satisfactorily and did not affect the performance of the current loop or the switching frequency filter. There were no interactions between the two loops that created stability problems. This result and the theoretical results of the inverter output current, with and without the VCL in chapters 3, 5 and 6, suggests that the two control loops (CCL &VCL) and the switching frequency filter can be designed separately.

Experimental values of the DC offset current component of 34 mA injected into the grid system (when supplying 500 W) was well above the 0.5% limit [4]. Therefore the problem of excessive DC offset current injected into the grid supply had to be solved if the use of power transformers is to be avoided and if all the objectives of this project are to be successfully completed. The corrective measures taken to minimise DC offset current needed to be cost effective and with insignificant power loss.

The results presented in this chapter have validated the new design process for a hysteretic current control, transformerless, unipolar inverter with a switching frequency filter for utility connected PV connections. The peak conversion efficiency of this transformerless inverter system implementing the theoretical design process developed in Chapters 3 to 6 was about 97%.

CHAPTER 8

REMOVAL OF D.C. OFFSET CURRENT

8.1. Introduction

The adverse effects of injecting DC current into the grid supply have been discussed in Chapter 2. In Chapter 7 it was also established that the transformerless inverter system designed and tested for this project would inject illegal magnitudes (i.e. greater than 0.5% of rated value) of DC currents into the grid supply. A new technique to remove DC offset current (DCOC) presented in this chapter is an expanded version of a paper presented by Sharma at IUPEC 2005 [69].

In applications where transformers are used between PV inverters and the grid network, the presence of high levels of DCOC in the primary side produces a unidirectional flux. This flux is additional to the bidirectional flux produced by the primary AC current and has the potential to increase core losses [45] and to degenerate the quality of the power supplied to the grid system. Experimental work has been carried to demonstrate this effect and the results are published in Appendix B. Therefore, whether a power transformer is used or not, it is of significant advantage in terms of the quality of power supplied by inverters, and in terms of power losses, that a method be developed to remove any DCOC. The technique to remove the DCOC must be simple, cost effective, and suitable for use with all inverters connected to the grid system.

To be able to remove or limit the DCOC, small magnitudes of DC current must be separated from relatively large magnitudes of AC currents. In this chapter it is shown that irrespective of its source, the DCOC can be separated from the AC current and

maintained below the acceptable limits without sacrificing the overall conversion efficiency of the inverter system. Simulation and experimental results are presented to show that the proposed cost effective technique can be used without compromising the dynamic response of the current feedback loop. Measured values of the DCOC injected by the inverter with and without the use of the new DC control loop are also presented to demonstrate that the DCOC injected into the grid supply was maintained at approximately zero.

8.2. DC Current Controller Specifications

To be able to remove the DCOC present in the output of the inverter it first has to be measured. There are three important conditions that need to be met when measuring the value of the DC current component. These are: -

a) the circuit designed to measure the DCOC must not introduce any additional offset current. This could lead to either over or under correction of the DC offset error, making it difficult to maintain the error at zero.
b) the measurement process should be able to carry out total separation of the DC current from the AC current. Failure to do so will prevent total removal of DCOC and may affect the ability of the current controller to accurately follow the reference current.
c) the proposed DC controller must achieve DC current attenuation without compromising the overall efficiency, the cost and the size of the inverter system. Failure to do so will compromise the benefits of avoiding the use of transformers and may make the design of the DC controller a pointless exercise.

To minimise power loss, the inverter outer loop resistance is always made as small as practically possible. Masoud and Ledwich [57] have established that this small value of resistance was sufficient to allow the use of a simple RC circuit arrangement to provide adequate voltage feedback, to reduce the DC offset current. The advantage of this method of measuring the DC voltage (due to the DC offset current) was that it did

not introduce additional DCOC. The disadvantage of the approach used by Masoud and Ledwich [57] was that it failed to provide adequate separation of the DC voltage from the AC voltage despite using an integrating stage with the RC circuit. However, in the present project, total separation of the DC voltage from the AC ripple voltage is required. Failure to do so may result in unacceptable magnitudes of DCOC being injected into the grid system. The aim of the DC controller designed in this section is to achieve total separation of the DCOC from the AC current, and hence its total removal.

8.3. Measurement of DC Offset Current.

Measurement of DC offset current using an RC arrangement with a PI controller is shown in Figure 8.1. The use of the PI controller instead of the P type controller used by Masoud and Ledwich [57] was to ensure that the steady state error in the DCOC was maintained at approximately zero.

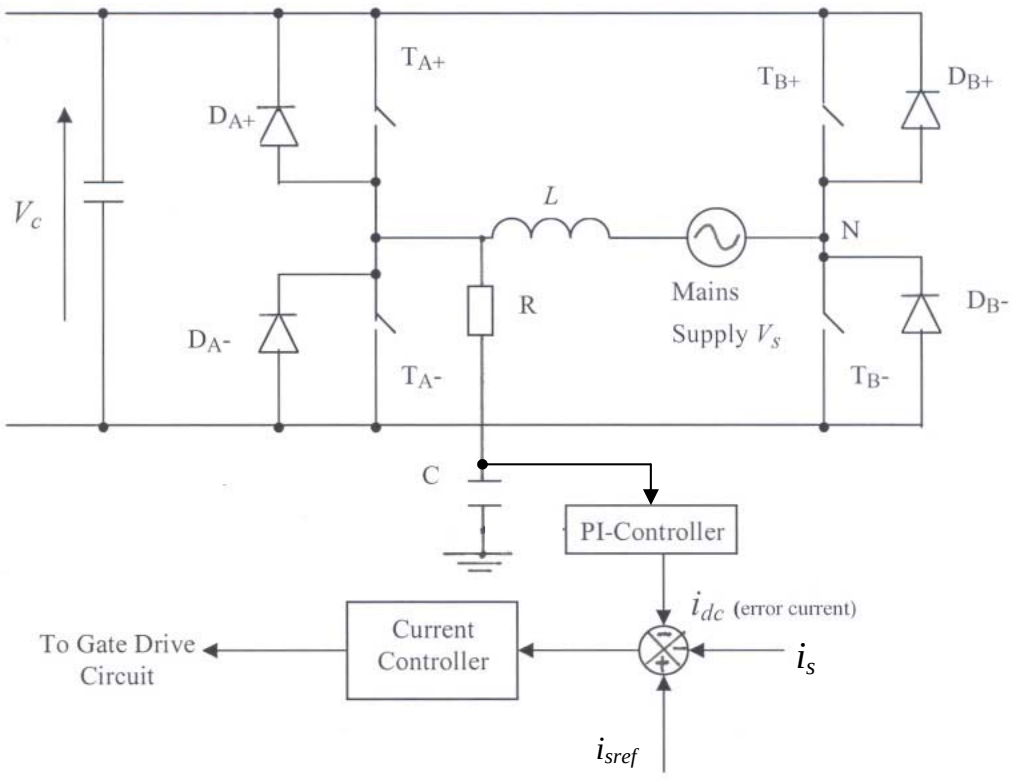


Figure 8.1: Measurement of DC offset current

The schematic implementation circuit for the PI-controller is shown in Figure 8.2. The transfer function of the PI-controller is given by:-

$$G(s) = \frac{K_{Pi}(s + 1/\tau_{pi})}{s}$$

Where $k_{Pi} = R_3/R_2$ proportional gain (Figure 8.2)

$\tau_{pi} = C_3.R_6$ integrator time constant (Figure 8.2)

The PI-controller includes a simple current limiter circuit to remove the potential for integrator wind-up. Wind-up is likely to occur if the rate of integration exceeds the feedback system response. This condition may lead to the PI-controller exceeding the saturation limit of the IC4 (Figure 8.2).

The upper current limiter circuit comprises of IC2, R_7, C_4 and D1 is responsible for keeping the output of the integrator below the preset value set by R_{11}. Similarly, IC3, R_8, C_5 and D2 are responsible for keeping the output of the integrator above the preset value set by potentiometer R_{12}. During normal operation, diodes D1 and D2 are reverse biased and the current limiting circuits plays no part in the operation of the integrating process. If on the other the output of the integrator tries to go above the positive limit set by R_{11}, the output of IC3 will drop quickly from its saturated value (positive supply rail) because the value of C_4 is relatively small. The output of IC3 will remain at the diode forward voltage drop value as long as the DC offset error is above zero. As soon as the error goes below zero, D2 becomes reversed biased and the integration process resumes. During this period IC4 remains saturated near the negative supply rail forcing D1 to remain reversed biased. The operation of the lower current limiter can be explained in a similar manner.

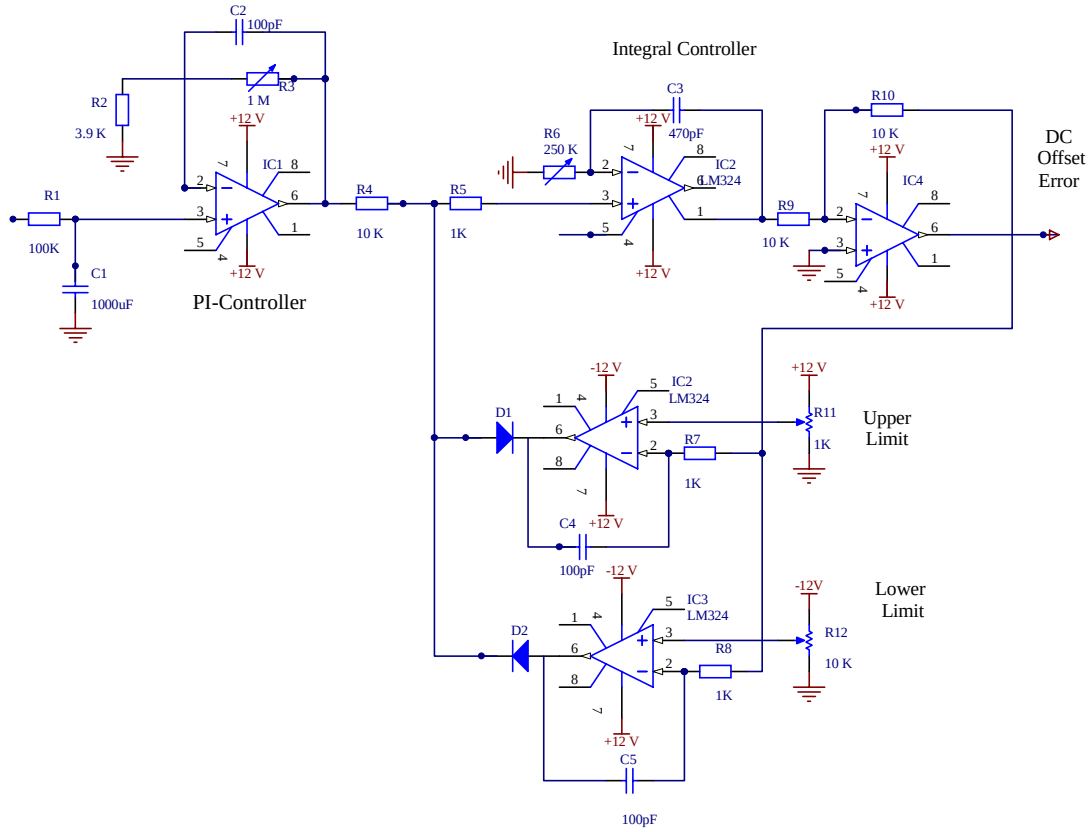


Figure 8 2: Implementation circuit for PI-Controller

The PI controller was tested separately and the output current shown in Figure 8.3 has an AC ripple component together with a DCOC component. The presence of this significant AC component introduced error in the reference current and therefore needed to be removed if the DCOC was to be maintained at acceptable levels.

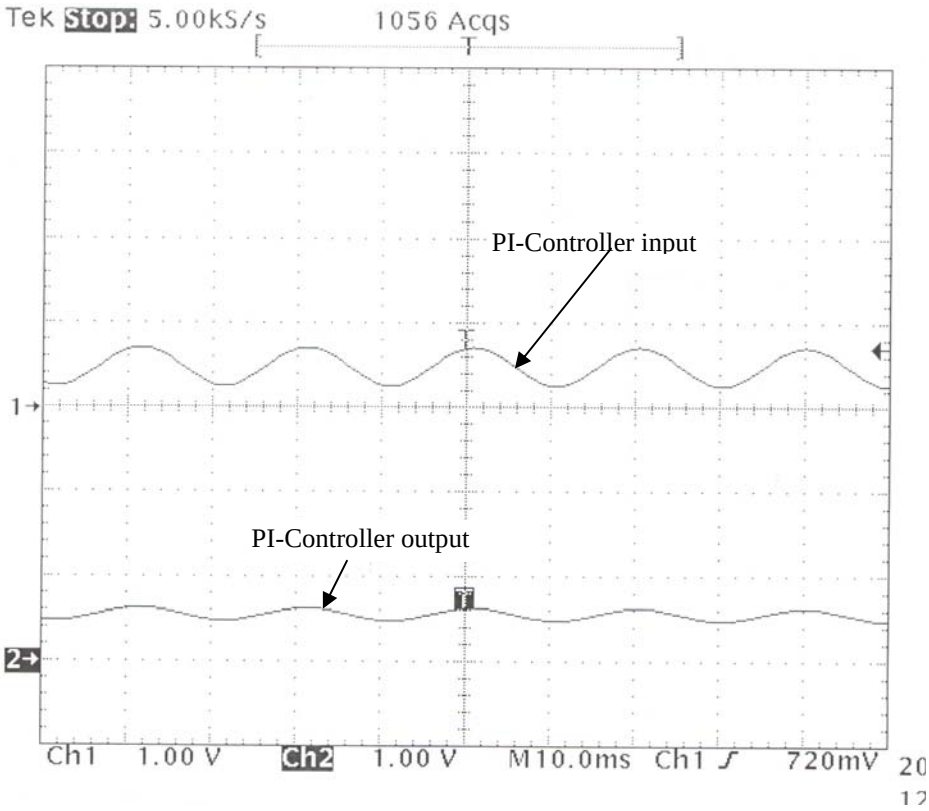


Figure 8.3: PI-Controller test results

8.4. Removal of AC Ripple Current

With reference to Figure 8.4, it was envisaged that adding a small voltage transformer (VT) with a 1:1 turns ratio connected before the PI controller could solve the AC ripple voltage problems. However, the simulation result illustrated by Figure 8.5 shows that the phase shift due to the 10 mH inductance *L* and the RC circuit (Figure 8.1) prevented perfect cancellation of the AC ripple. Therefore, a small AC voltage component is present at the capacitor terminal.

To minimise stability problems, simulation of the inverter system with the DC current controller needed to be carried out before implementing the schematic circuit shown in Figure 8.4. This is presented in the next subsection.

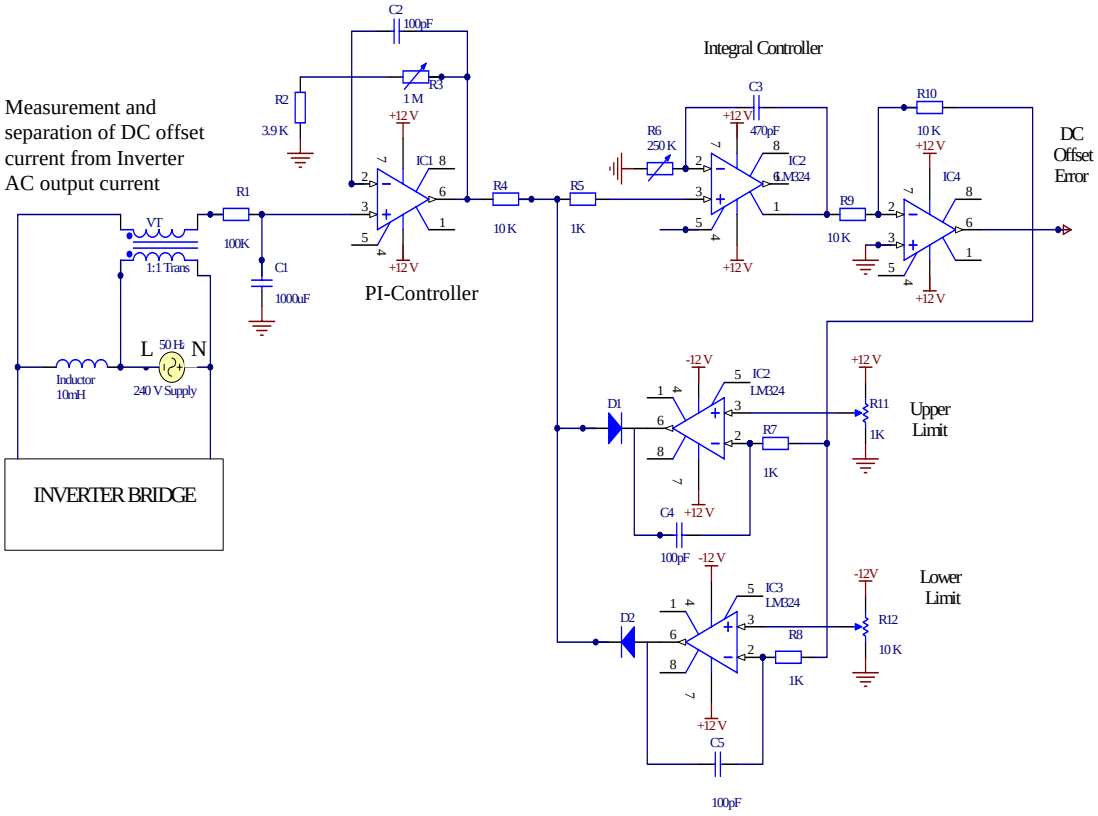


Figure 8.4: Implementation circuit for DC offset current controller

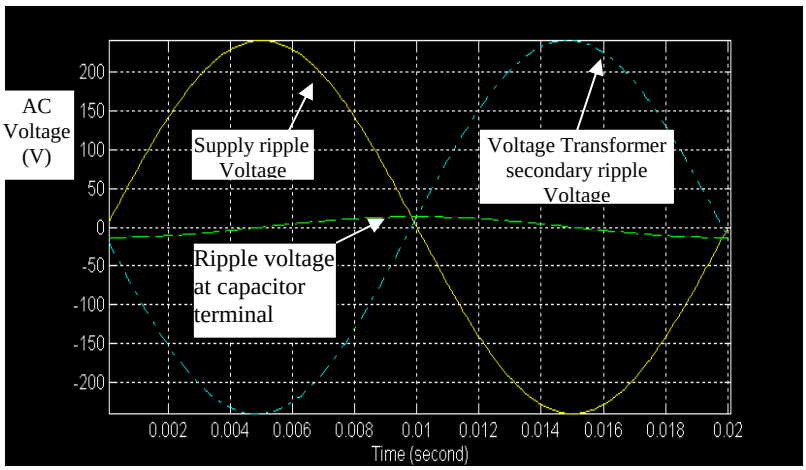


Figure 8.5: Ripple voltage cancellation

8.5. Simulation Results

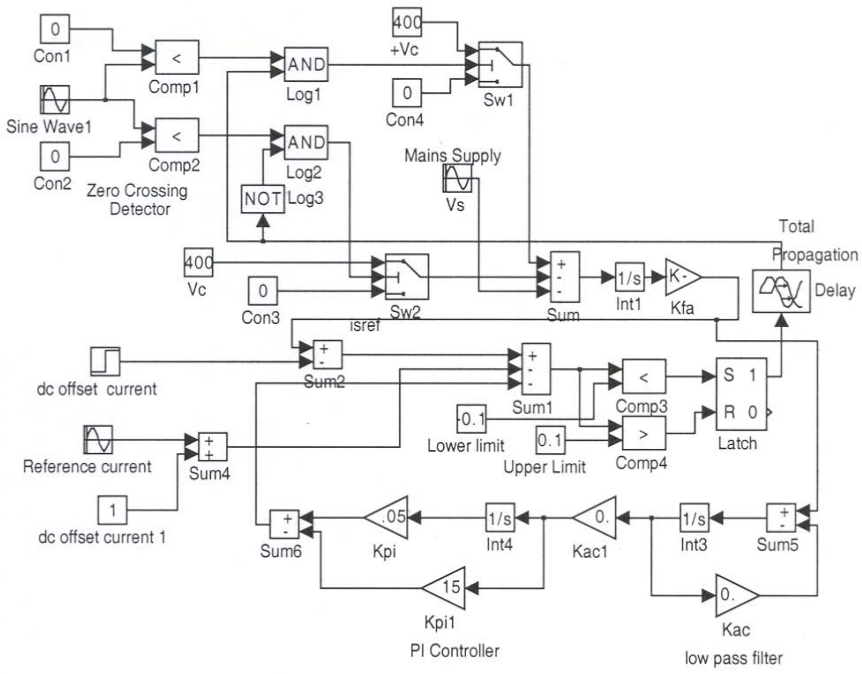


Figure 8.6: SIMULINK model of current loop with DC removal loop

In Chapters 3 to 6, the results of the theoretical analyses of the control loops, and the simulation results using SIMULINK models were both analysed before proceeding with experimental work. Analytical analyses of the complete inverter control systems are very complex and difficult to carry out. It was decided, based on the close correlation between theoretical analyses and SIMULINK simulation results presented in chapters 3 to 6 that using only the SIMULINK method for the current controller and the DC offset current controller, was sufficient.

The SIMULINK model of the CCL shown in Chapter 3, Figure 3.15 was modified to include the DC offset current control loop (Figure 8.6). The purpose of using this model to obtain simulation results was to establish if the inclusion of the DC offset current control loop gave rise to any stability problems. Reasonable values for the proportional and integral gains of the PI controller were chosen to limit overshoot and achieve acceptable settling time. A step increase of 2 A DC offset current was applied 0.05 seconds after the inverter system was turned on. The responses of the current

controller and the PI-controller, when subjected to such extreme variation in DCOC (+2 A), are shown in Figures 8.7 and 8.8 respectively. These simulation results indicate no stability problems with the addition of the DC offset current control loop. These results provided the platform for the experimental tests to proceed.

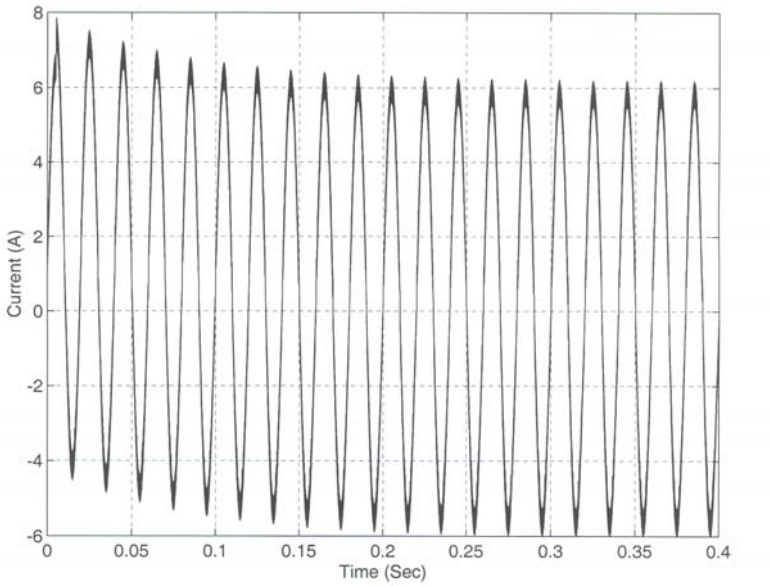


Figure 8.7: Inverter output with DC offset correction

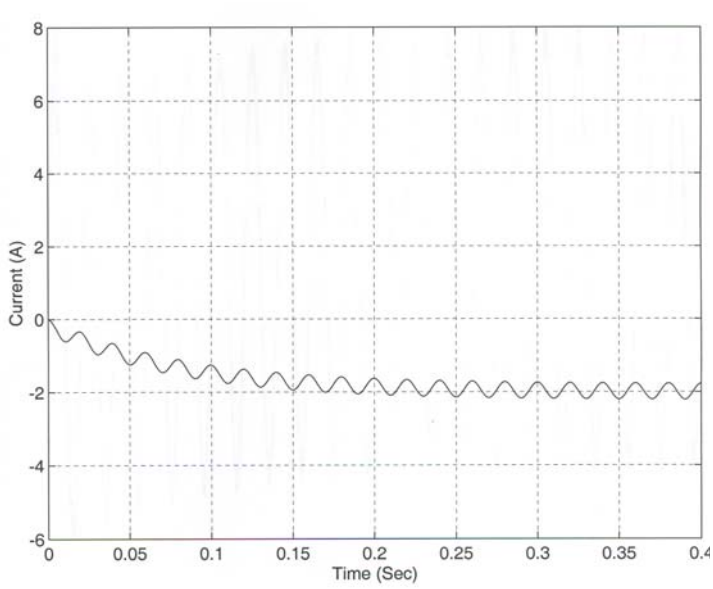


Figure 8.8: PI-Controller output current

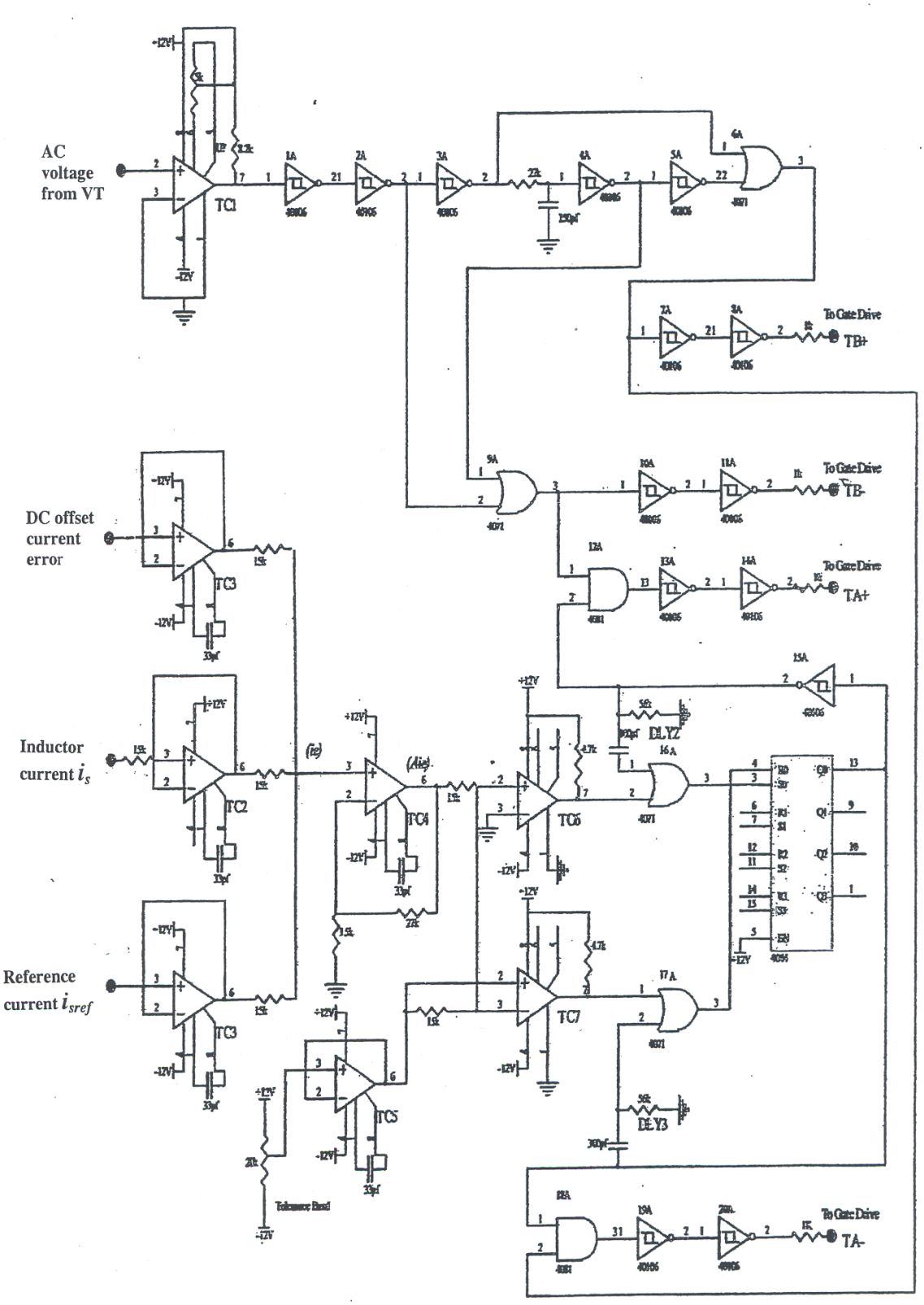


Figure 8.9: Schematic diagram of CCL with DC offset current controller

8.6. Experimental Results

The complete CCL with the DC offset current controller was designed and constructed. As shown in Figure 8.9, the DCOC error from the DC controller is the third input of the current controller circuit. The inverter output current was varied and the DC component injected into the grid system from the inverter output was measured.

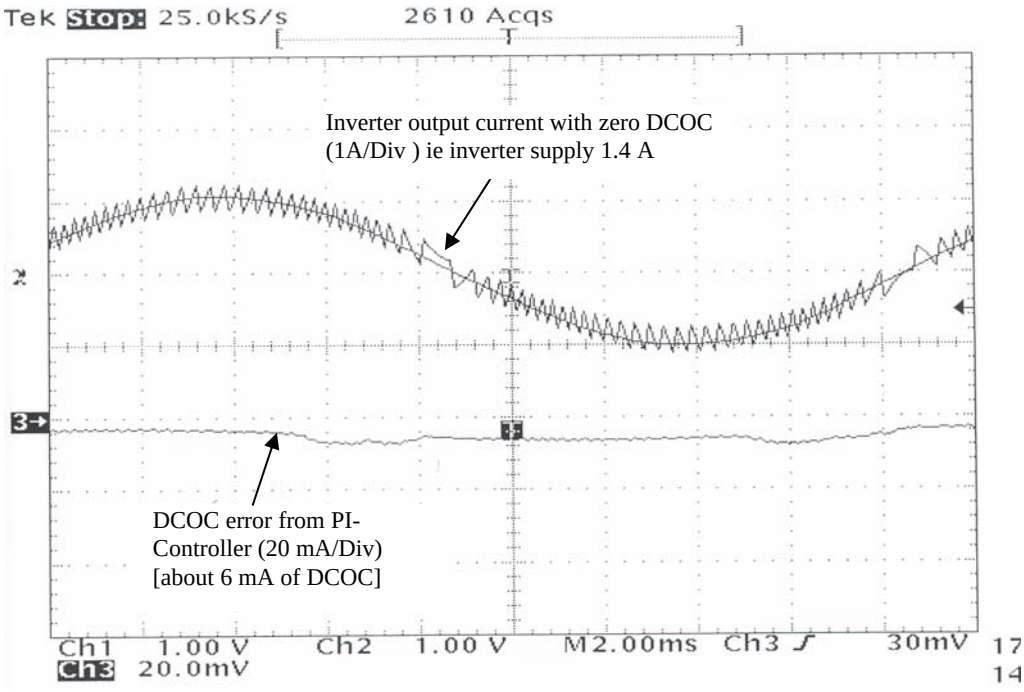


Figure 8.10: PI-controller and inverter Output Current

Experimental results for the output current of the unipolar switched inverter supplying about 500 W to the grid system is shown in Figure 8.10. With the use of the VT (Figure 8.4) the output from the PI controller is ripple free. This result tends to suggest that if L is small then phase shift is not an issue. When the inverter output power was increased from 0 to 500 W the DCOC injected into the grid remained approximately zero. The DC offset current controller was then disabled and the inverter tested under the same load conditions. It was found that without the DC controller, the DCOC injected into the grid system varied between 16 mA and 28 mA.

The inverter was tested several times with and without the DC controller and in all cases removal of the DC offset current was achieved. The additional component cost for the DC offset current controller is less than $30.

8.7. Conclusions

A new technique to remove the DCOC from the output of a unipolar, current control, transformerless PV inverter for utility connection has been realised.

Experimental results have been presented to show that if the inductance of the current loop is small zero DCOC can be maintained irrespective of its source. The proposed DC current control method is cost effective and does not have any adverse effect on the dynamic response of the current controller. The removal of the DCOC has been achieved without sacrificing the overall conversion efficiency of the inverter system.

This DC control technique can also be used in bipolar switched inverters and in inverter applications where transformers are used to improve the quality of power fed to the grid network.

Since this new method of removing DCOC has been successfully achieved, the cost benefits derived from transformerless PV inverters for utility connection systems include the following:-

- Savings in cost of a 1.2 kVA power transformer which is about $300.

- Typical measured values of power loss for a 1.2 kVA transformer suitable for utility connected PV inverter application were found to be about 50 W of which 22 W was fixed loss. These figures were obtained from open-circuit and short-circuit tests carried out on the 1.2 kVA transformer. The additional solar panel capacity at about $6/W required to overcome the transformer losses in this case was about $300.

- In the above example the measured value of fixed losses was 22 W. The removal of the fixed losses allows lower levels of power to be injected into the grid.

CHAPTER 9

CONCLUSIONS AND RECOMMENDATIONS

9.1. Introduction

In this chapter a brief summary of the most important findings of this thesis and their significance in the design of a hysteretic current control, transformerless, unipolar switched inverter for utility connected PV system is presented. The chapter concludes with some suggestions for further improvement of the quality of the power delivered by such PV inverters.

9.2. Major Outcomes of Research

The main aim of this thesis was to present a design procedure for a PV inverter system suitable for grid connection that would lead to:-

- higher inverter conversion efficiencies
- improved output power quality and
- reduced capital cost.

Theoretical and experimental results presented in this project validate a new design process for a transformerless, 1 kW single-phase, unipolar switched PV inverter system that achieves these objects. A brief summary of the work presented in this thesis and the major outcomes arising from it are as listed below.

a) **Inverter Design Outcomes:**

- New theoretical models have been developed that yield component values, and allow the estimation of switching frequencies along the current waveform for unipolar and bipolar switched inverters. Inverters cannot be constructed with zero circuit delays and the benefit of these models is that they include delay. Also key parameters such as V_c, L and I_{Tol}, obtained using the design equations, are more realistic because they include delay, making it easier to achieve desired inverter specifications.

- The main technical contribution is undoubtedly the development of new theoretical models to explain why implementation delays are responsible for greater current distortion and hence for the generation of switching frequency harmonics in unipolar switched inverters compared to bipolar switched inverters. The theoretical analyses also revealed that there were three current loop parameters, V_c, L and t_d that influenced the level of low frequency harmonics generated by unipolar inverters. These three variables together determine the magnitude of the low frequency odd harmonics. Consequently, implementation delay cannot be ignored when designing unipolar switched inverters, as it affects the power quality and the efficiency of the inverter system. This outcome is useful for designers intending to take advantage of the benefits of unipolar switched inverters, outlined in Chapter 2.

b) Efficiency Improvements:

- The peak conversion efficiency of the transformerless PV inverter system using the new design process developed in Chapters 3 to 8 was about 97%. Efficiency was obtained by measuring the instantaneous input and output power. It has been suggested by Calais et al [17] that efficiencies around 96% were achievable for transformerless inverters. Therefore, the efficiency of about 97% achieved in this project is good.

c) Cost Reduction:

- A reduction of about 20% in capital cost of the PV inverter system has been achieved:
    i. by eliminating the 1 kW power transformer, and
    ii. in the savings associated with not providing additional PV capacity to overcome transformer losses.

These savings were calculated after deducting the extra cost of providing a DC offset current control loop and the switching frequency filter.

d) Power Quality Improvements:

- An important technical contribution is the development of an original split inductor AC filter arrangement that minimised EMI generation, prevented unwanted inverter switching and attenuated switching frequency current harmonics. The use of this split inductor arrangement allowed the magnitude of the switching frequency current harmonics injected into the grid network to be maintained at negligible levels (Figure 5.9, Chapter 5).

- Experimental results presented in this thesis have established that transformerless PV inverter systems can inject illegal magnitudes of DC offset current into the grid system. Therefore, the successful design of a new cost effective and efficient DC offset current controller was an important contribution without which it would have not been possible to have transformerless PV inverters connected to the utility supply.

9.3. Review of Research

The justifications and the benefits of carrying out research to improve the efficiency and the power quality of utility connected PV system are outlined Chapter 1. The project objectives and a summary of the strategies to achieve these objectives are also included in this chapter.

A comprehensive review of relevant literature is presented in Chapter 2. The key findings from this review can be summarised as follows:-

- While the potential benefits of improved efficiency associated with unipolar switched inverters have been realised by others, there is an absence of published information related to the quality of power supplied by such inverters. It was clear from the review exercise that the quality of power injected into the grid was a critical issue that required further investigation if the aims of this project were to be achieved.

- It was difficult to find evidence of publications that included the relationship between implementation delays, generation of low frequency current harmonics and efficiency of unipolar and bipolar switched inverters.

- There was no published evidence that the magnitude of current harmonics generated by hysteretic current control unipolar switched inverters could be economically and efficiently maintained within the limits specified by Australian Standard AS4777.2, 2005.

- In Australia some power authorities allow up to 10 kW transformerless PV inverters to be connected to their grid network. However, no evidence was available to confirm that DC offset current injected into the grid system by transformerless inverters could be economically and efficiently maintained within the limits specified by Australian Standard AS4777.2, 2005.

9.3.1. CCL: Theoretical Design

In chapter 3 a new theoretical model for determining the switching frequencies along the current waveform of a hysteretic current control unipolar switched inverter system has been successfully developed. The new aspect of this model of the current loop was the inclusion of implementation delays. Including delays in the design process produced more realistic numerical component values of the current loop. The component values chosen using this procedure allowed maximisation of the inverter efficiency without compromising the quality of inverter output power.

For a given switching frequency band and total harmonic distortion under the same load conditions, 50% less inductance for the current loop is required in the unipolar switching mode, compared to the bipolar switching mode. Consequently, less copper is required for unipolar switched inverters resulting in lower cost and lower power losses.

The theoretical results presented in Chapter 3 show that unwanted implementation delays give rise to an unacceptable level of distortion of the inverter output current (Figure 3.24) around the zero crossing, and hence limits the minimum value of AC filter inductance that can be used in the current loop. Therefore, there is a trade off between circuit delays and the efficiency of the inverter system.

In Chapter 3 results are also presented to show that implementation delays are responsible for the low frequency harmonics generated by hysteretic current control unipolar switched inverters. A new theoretical method to determine average value of the inverter output current has been developed to explain why these low frequency harmonics are generated in unipolar switched inverters but are absent in bipolar switched inverters. It was established in Chapter 3 that the fixed term in equation 3.41, that formed approximately a square wave with amplitude of $\approx\left(\frac{t_d V_c}{2L}\right)$ was responsible for the low frequency harmonics.

Finally, it was established (equation 3.23) that the switching frequencies along the current waveform (and hence distortion) can only be controlled by the tolerance band if I_{TOL} was significantly greater than $V_C\left(t_d / L_2\right)$.

9.3.2 CCL: Practical Implementation

The circuits for the current loop for a utility connected 1 kW unipolar switched inverter system, based on the design procedure developed in Chapter 3 were successfully carried out in Chapter 4.

Experimental results presented for the current loop (Chapter 4) demonstrate that the output of unipolar switched inverters can be made less susceptible to internal switching noise. There are four equivalent switching options but only one of these options will lead to suppression of switching noise and eliminate the need for additional filters.

The use of a split inductor arrangement to minimise the influence of noise or voltage spikes (due to stray capacitance) produced when the polarity of the DC voltage changes is also presented in Chapter 4. This split inductor arrangement also sets the platform for the design of the switching frequency filter.

Finally, simple practical techniques have been presented to significantly reduce the circuit delays of the current controller.

9.3.3 CCL: Switching Frequency Filter

It has been demonstrated in Chapter 5 that the switching frequency harmonics can be successfully attenuated using an additional capacitor C_F, a damping resistor R_c (Figure 5.1) and the inductance L_2 which is part of a split inductor arrangement shown in Figure 4.3. As such, filtering is achieved without increasing the resistance of the inverter outer

loop and without sacrificing the overall conversion efficiency of the inverter system. The use of the split inductor arrangement also makes the SFF a very cost effective method.

The stability and the performance of the current loop is unaffected by the new AC filter network provided the resonance frequency of the SFF is less than the minimum switching frequency of the inverter switches.

9.3.4 VCL: Theoretical Design.

A new design procedure for the voltage control loop that returned numerical component values for the voltage controller has been successfully carried out in Chapter 6. A table (Table 6.1) was developed using this design procedure to allow designers to choose values for the capacitor C, the time constant of the low pass filter τ_{fc} and the proportional gain K_p to achieve acceptable DC input voltage regulation, and to maintain the level of the third harmonic current I_{s3} within the limits specified by AS4777.2, 2005.

Results presented in Chapter 6 established that no significant difference in the level of harmonics generated between the PI controller and P type controller existed to prevent the P-controller being used in the unipolar switched inverter designed in this project.

The theoretical results using the SIMULINK model of the VCL presented in Chapter 6 also illustrate that the steady state characteristics and the transient response of the VCL using the P-controller are acceptable and meet the desired specifications

Finally, there are no interactions between the voltage and the current controllers that prevent the two controllers from being designed separately.

9.3.5. VCL: Experimental Results.

The construction of the circuit for the VCL with its proportional controller was reported in Chapter 7. The maximum difference in the steady state error in V_c at rated current between the experimental and the theoretical was 4%. This small difference was expected because the supply impedance was ignored, and it was difficult to measure VCL components accurately.

It was also established in Chapter 7 that the measured values of the DC offset current component injected into the grid system were well above the maximum limit specified by Australian Standard AS4777.2, 2005. Therefore the problem of excessive DC offset current injected into the grid supply had to be solved if the use of power transformers was to be avoided and if all the objectives of this project were to be successfully completed. The corrective measures taken to minimise the level DC offset current injected into the grid network are cost effective, and with insignificant power loss.

9.3.6. DC Offset Current Controller

A new technique to remove the DC offset current from the output of a unipolar, current control, transformerless PV inverter for utility connection has been realised.

Experimental results have been presented in Chapter 8 to show that approximately zero DCOC can be maintained irrespective of its source. Since the inductance of the current is always small to minimise inverter losses, phase shift may not be a problem. The proposed DC current controller was cost effective, and did not display any adverse effect on the dynamic response of the current controller. The removal of the DC offset current has been achieved without sacrificing the overall conversion efficiency of the inverter system.

This DC control technique can be used in bipolar switched inverters and also in inverter applications where transformers are used to reduce distortion of the magnetising current.

Since this new method of removing DC offset current has been successfully achieved, the benefits derived from transformerless PV inverters for utility connection systems have been realised.

To verify the aims of the project, the design, construction and testing of a hysteretic current control unipolar switched inverter system for PV application have been successfully completed.

In conclusion, this thesis has presented theoretical and experimental results to validate a new design procedure for a transformerless unipolar switched inverter connected PV connections. The inverter system is a technically proven low cost, high conversion efficiency system to convert the DC currents from solar panels to a high quality sinusoidal current for grid applications.

9.4 Applicability of Results and Design Process

Equation 3.23 developed in Chapter 3 to determine the frequencies along the inverter output current waveform, are applicable to unipolar switched inverters of any power ratings. Equations 3.24, 3.25, and 3.26 (derived from equation 3.23) to estimate key switching frequencies F_{min}, F_{med} and F_{max} respectively, can also be used to design unipolar inverters of any power rating.

In this project, estimation of low frequency harmonics is achieved by using equation 3.42 (Chapter 3) and by using the SIMULINK model of the current loop. A comparison of the low frequency harmonics results show that using equation 3.42 is suitable for inverters with a rating of 1.5 kW or less. Above this rating, the term $(-\omega t_d \hat{I}_{sref} \cos\theta)$ in equation 3.40 cannot be ignored. To determine magnitude of low frequency harmonics for inverters with a rating greater than 1.5 kW, the FFT of the average current i_{av} using equation 3.40, or the SIMULINK model of the current loop should be used.

The 100 Hz ripple present in the DC current I_y contributes to presence of third harmonic current at the inverter output. The VCL design process presented in Chapter 6 allows inverter designers to use equation 6.23 and Table 6.1 to choose VCL parameters such that the magnitude of this third harmonic current is minimised.

9.5. Implications of Project Outcomes

The implications of the outcomes of this project in promoting grid connecting PV generation in Australia can be summarized as follows:-

- it allows designers to select inverter parameters such that the quality of the power fed into the grid supply system, by transformerless PV inverter, remains within the levels specified by Australian Standard AS 47772.2, 2005.

- it confirms that unipolar switching can be used in transformerless PV inverters. This is despite the unipolar mode being responsible for the generation of low frequency harmonics. Therefore, the benefits of using unipolar switching presented in Chapter 2, can be realised.

- it allows the use of transformerless PV inverters for grid connection and hence a reduction in the cost of PV systems. It was shown in Chapter 7 that without the use of the DC offset current controller the DC fed into the grid was above the limits specified by Australian Standard AS 47772.2, 2005

- it confirms that DC offset current controllers can also be used in inverters that use power transformers to improve the performance of the transformers.

9.6. Recommendations for Further Work.

In this project, the magnitude of current harmonics injected into the grid system by the unipolar switched inverter designed for a 1 kW domestic PV application is within the present limits specified Australian Standard AS 4777.2, 2005. Therefore the generation of low frequency current harmonics is not an issue. However, there are situations outside the scope of this project where the generation of low frequency harmonics may be of concern. These include:-

- In a distributed generation with a large number of single phase PV inverters connected to the grid system, (e.g. the 665 Solar Olympic Village homes project in Australia), the summation of the low frequency harmonics may be a problem for the supply authorities.

- As the Australian Standard becomes more stringent to combat pollution of power supply systems, concerted effort will be required to minimise the detrimental distortion of the supply voltage and current by non-linear loads such PV inverters.

Therefore, potential avenues to further reduce generation of low frequency harmonic currents by unipolar switched inverters require investigation. One of the options that can be investigated is to use a modified hysteretic current control. The hysteretic current control used in this project relies solely on the inverter output current going outside a preset tolerance band to change the state of the inverter switches. Investigations need to be carried out to establish if adding the turn-on and turn-off durations to the existing decision making process to change the state of the inverter switches will lead to an improvement of the minimum switching frequency. Preliminary work carried out to test this idea is included in Appendix C. So far it has proved very difficult to make the area

above and below each switching cycle equal, near the zero crossing (Figure 3.22, Chapter 3).

9.6.1. Variable Reference

A fixed DC input voltage V_c was used in this project. In Australia, the supply voltage V_s can vary by as much as 36.8 V between the upper (243.8 V) and lower (207 V) legal limits. A cost benefit analysis for keeping the ratio (V_c/V_s) constant needs to be investigated. Additional cost will be incurred to modify the VCL to provide a variable reference voltage such that V_c is adjusted as V_s changes to keep the ratio (V_c/V_s) constant. The potential benefits of this would be reduced switching losses, and lower current distortion near the peak value of the output current. It is envisaged that measuring the switching loss (in the tens of mW range) would be difficult aspect of this exercise.

9.6.2. Replacement of Voltage Transformer in DC offset Current Controller

In Chapter 8, the use of a voltage transformer (VT) allowed successful separation of and removal of small magnitudes of DC offset current from large magnitudes of AC current fed into the grid supply by a PV inverter system. This result demonstrated that the use of power transformers can be avoided and hence an important objective of this project was achieved.

However, to further reduce cost of the DC offset current controller investigations are continuing at University of Southern Queensland to find other simpler methods that do not require the use of the VT. The use of RLC networks is being investigated.

9.6.3. Control Circuits and Reliability Tests

The purpose of the analog control circuits developed in this project was to validate the new design procedures for the control loops. On completion of the investigations that are extensions of this project (presented in sections 9.6 and 9.6.2), the technology used to implement these control loop circuits will need to be reviewed. For example, the cost of the simple analog gate drive circuits and the inverter bridge designed was less than A$200. However, the performance of these component of the CCL, needs to be compared with the new commercially available inverter bridge with matching digital gate drive modules (with in built protection) that cost between A$600 and A$700 for reliability. Similarly, the use of software to make all intelligent control decisions associated with the VCL, SFF and the DC control loop needs to be investigated.

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APPENDIX A

MAXIMUM POWER POINT TRACKER AND DC TO DC CONVERTER

1.0. Introduction

The maximum power point tracker (MPPT) and the DC to DC converter, while they are not the main focus of this thesis, have been briefly discussed in Chapter 2. However, it is necessary to describe the circuits developed to perform the maximum power tracking and the DC voltage step-up functions. Therefore experimental results associated with the performance of the MPPT and the boost converter are presented in this appendix and not in the main part of this thesis.

2.0. Gate Drive Circuit

The circuit schematic of the optocoupler isolated gate drive circuit used to switch the IGBT in the inverter-bridge is shown in Figure A1. The gate drive circuit has two primary functions. Firstly, it provides electrical isolation between the current controller circuits and the gate of the IGBT. Secondly, it amplifies the control signal from the Schmitt Triggers in the current controller so that it can provide adequate power to the gate of the insulated gate bipolar transistor (IGBT). This was done to ensure that the IGBTs are turned on and off such that minimum time is spent in the active region, hence keeping the instantaneous power dissipated by the IGBT to a minimum.

Transformer coupling offers several advantages such as impedance matching, DC isolation and either step-up or step down capability. Transformers however, can only deliver an AC signal since the core flux must be reset after each half circle. This property cannot be fulfilled in the proposed application because the duty cycle of each switching event is not 50%. Therefore, if a transformer is used in this application then there is a possibility of the secondary voltage exceeding the voltage rating of the components in the gate drive circuit.

Consequently, the optocoupler HP2400 was chosen. Its rise and fall times were 10 ns and 100 ns respectively. These times were considered fast enough:

a) to turn-on and turn-off the IGBT and keep instantaneous power dissipated by the IGBT to a minimum
b) to also keep the hardware delays to a minimum, so that the switching frequency could be controlled using the size of the tolerance band. If the circuit propagation delay is large the period of the maximum switching frequency is governed by delay rather than by the magnitude of the tolerance band.

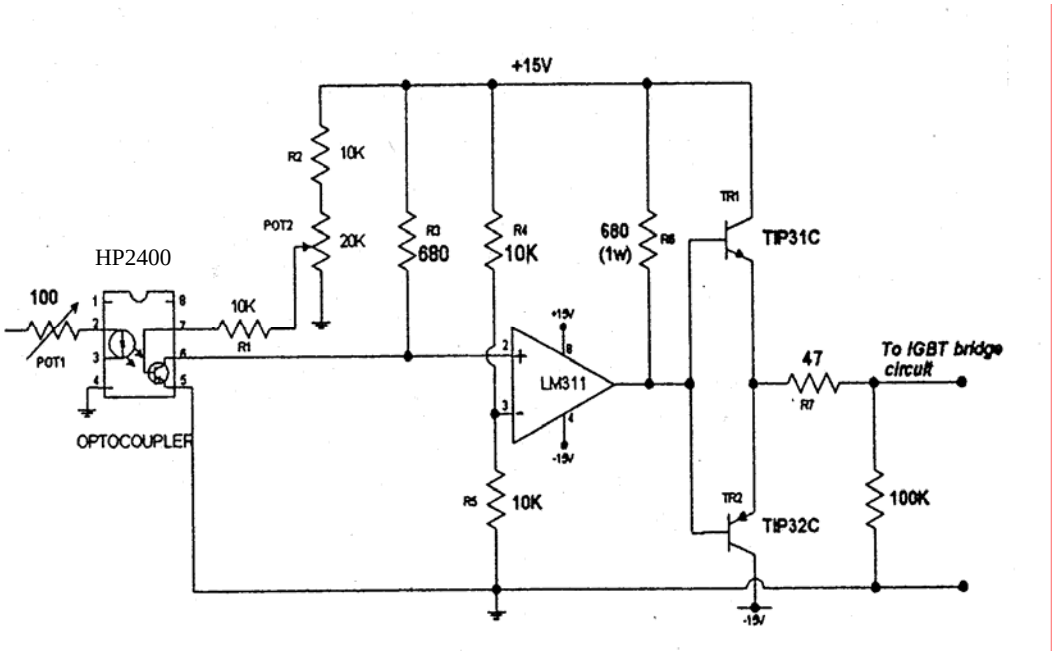

Figure A1: Gate drive circuit

The output of the optocoupler is fed to the comparator LM311, whose function is to control the switching of the *npn-pnp* totem-pole transistors TP31C and TP32C (Figure A1). For the IGBT (Q_5) in Figure A2 to turn on, the comparator turns off and hence transistor TP31C turns on and applies the +15 V source to the gate. The IGBT turns off when the –15 V source is applied to the gate through the 47 Ω resistor R_7 and transistor TP32C. The value of R_7 is small to ensure that fast turn on and off is maintained.

3.0. Boost Converter with Maximum Power Point Tracker

The solar panels, the maximum power tracker (MPPT) and the step-up DC to DC converter used are shown in Figure A2. As mentioned earlier, the DC to DC converter with its MPPT was not the main focus of this project. However, it had to be designed and constructed in order to determine the maximum possible efficiency that could be achieved and to test the inverter voltage and current controllers.

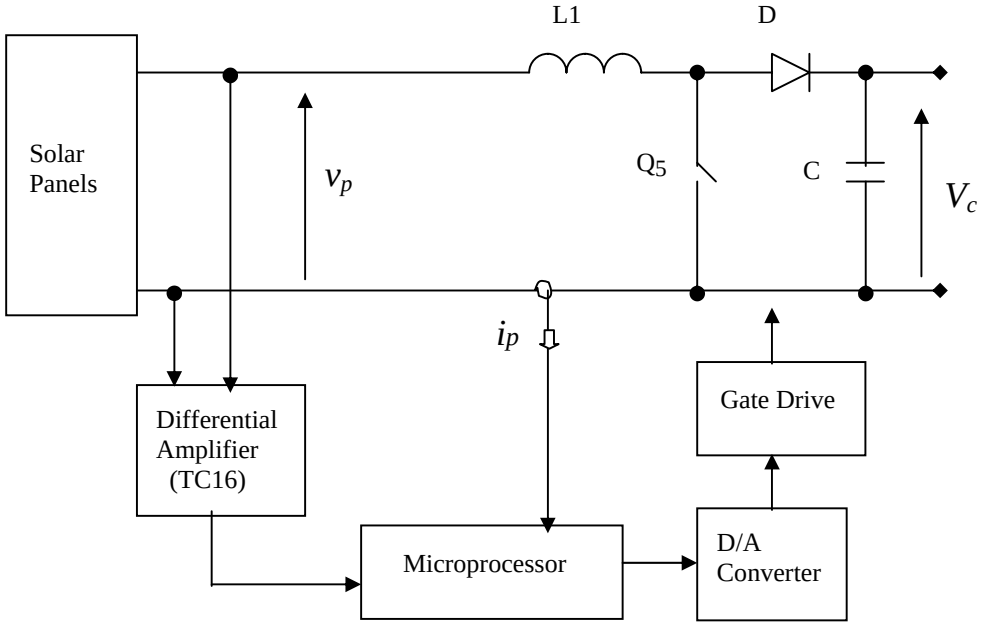

Figure A2: Maximum power point tracker and boost converter.

Depending on insolation level and temperature, the reference current is continually adjusted by the MPT so that optimum power is obtained from the panels. As insolation level or temperature changes, both v_p and i_p will change.

The MPT was designed using the Motorola M68HC11 microprocessor that has in-built A/D converters. The microprocessor required a properly designed 5 V power-supply. This was necessary because MC68HC11 is susceptible to fluctuating power supply voltages (V_{cc}) and cannot operate with V_{cc} much lower than 4.5 V. If V_{cc} drops too low then the CPU's operation may become erratic, potentially resulting in the device sending an incorrect switching command to Q_5.

Panel voltage (v_p) is stepped down by differential amplifier TC16, which is buffered by a voltage follower and then fed to the input of the A/D converters. The panel current (i_p) is sensed by a Hall Effect sensor, which provides as output a voltage proportional to the current. This output voltage is connected to one of the microprocessor A/D converters. The microprocessor output is a voltage proportional to the reference current i_{pr} through an external D/A converter. During normal operation the microprocessor continuously executes the maximum power-tracking program that resides in its memory. The maximum power-tracking algorithm is briefly described below.

Step 1:

- Set $i_{pr} = \Delta i$ (Δi = 0.02 A). This is the smallest increment by which i_{pr} can be changed)
- Set P_{old} (= old panel power) to zero

Step 2:

- Read v_p and i_p; Calculate new panel power = $P_{new} = v_p\ i_p$; calculate power difference $P_{diff} = P_{new} - P_{old}$; replace P_{old} by P'_{new} . If $P_{diff} > 0$, then change i_{pr} by

1 increment in the same direction as that of the previous change otherwise change i_{pr} by 1 increment in the direction opposite to that of the last change.

Step 3 :

- Go back and do step 2

At steady state, the above algorithm results in i_{pr} oscillating by ±0.02 A about its optimum value. The peak current out of the experimental PV system is 4.5 A. An efficiency of more than 99 % is therefore achievable.

The current controller for the boost converter provides the switching signals for IGBT Q_5 so that i_p, the output current from the panels, is forced to stay within a small tolerance band around the reference current i_{pr}. When Q_5 is on, diode D is reverse biased and hence i_p increases. When Q_5 is turned off energy is transferred from the solar panels and inductor L_1 to capacitor C and the inverter. As mentioned in Chapter 2, capacitor C should be large enough to keep the ripple content of voltage V_c within acceptable limits.

4.0. Experimental Results

To test the MPT, the inverter system was replaced by a constant voltage source as shown in Figure A3. This closely resembled the practical conditions since under normal operating conditions the capacitor voltage would be maintained at a constant value by the inverter control system.

Two groups of solar panels mounted on the same supporting frame were used to verify the performance of the MPT. Each group was made up of 7 x 75 W series connected panels. The output of the first group was connected to a resistive load so that it could be manually adjusted to extract maximum power throughout the test period. The second

group formed part of the test circuit shown in Figure A3. The result obtained is shown in Figure A4.

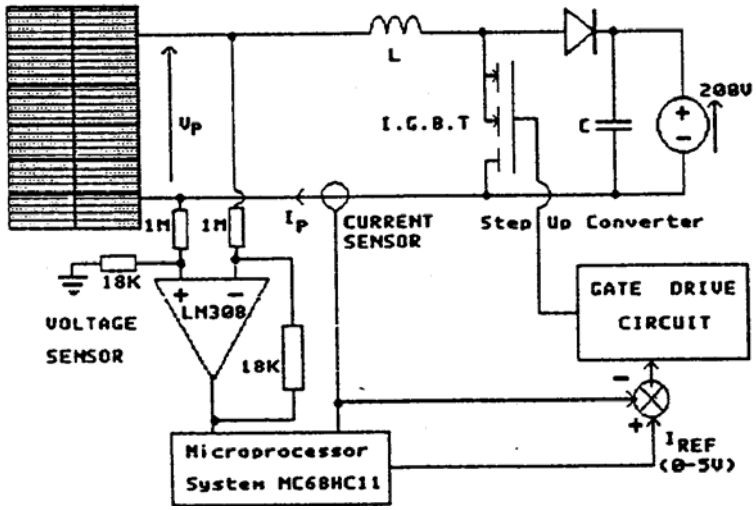

Figure A3: Test circuit for MPPT.

There was a discrepancy of about 2% on the average output power between the two groups of panels. It was discovered that the 7 panels operating without the MPPT were slightly more efficient than the manually controlled group of solar panels. Another reason for the discrepancy was that the output current from the group without the tracker was pure DC whereas the current from the other had a ripple component of ± 0.05 A.

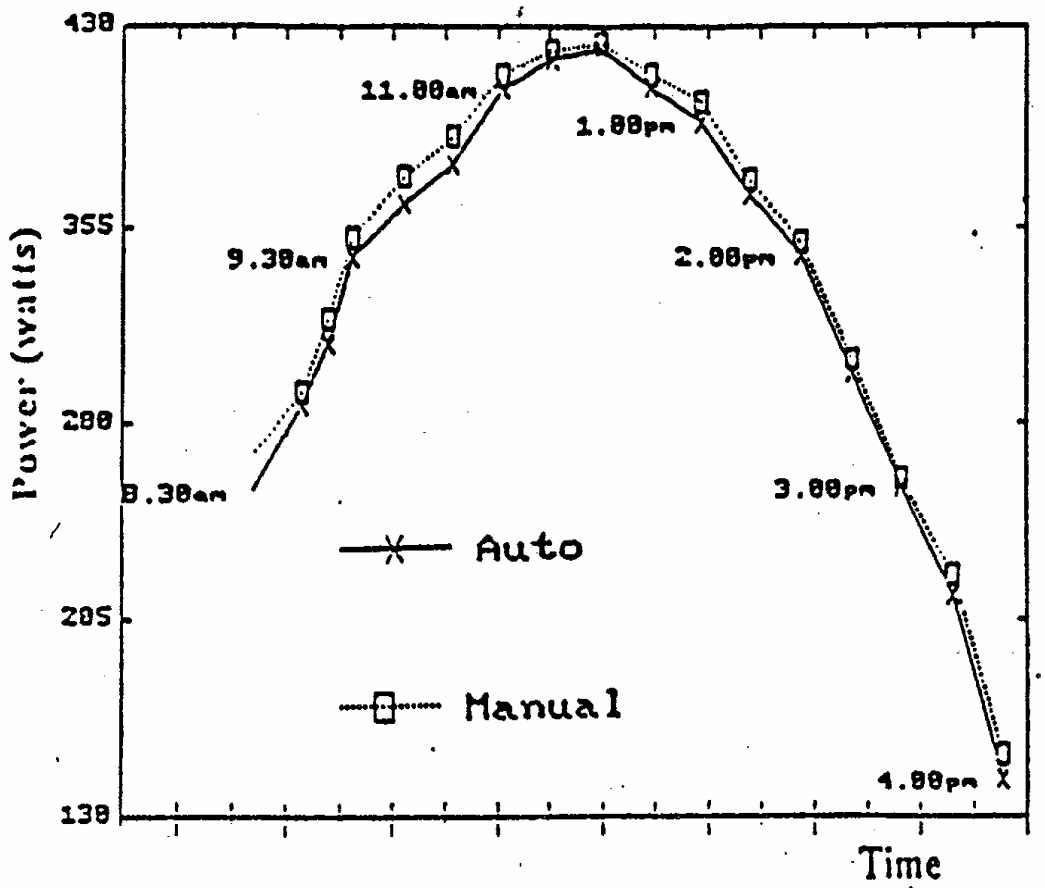

Figure A4: MPPT Test Results (Auto: with MPPT, Manual: without MPPT)

5.0. Conclusion

The MPPT and the boost converter were successfully constructed and tested. An efficiency of about 98% for the MPPT, and an overall efficiency of about 97% for MPPT together with the boost converter were achieved. These results were published by Sharma and Bowtell [22]. It was difficult to economically achieve any further increase in

efficiency, and as this stage of the inverter system did not directly influence the quality of the power injected into the grid supply, it was not included as the main focus of this project.

APPENDIX B

EFFECT OF DC OFFSET CURRENT ON POWER TRANSFORMERS

1.0. Introduction

PV inverters that are connected to the grid via transformers do not inject DC offset current into that supply system. However the presence of DC current at the output of the inverter (secondary side of the transformer), can lead to several adverse effects on the transformer. These effects depend on the transformer construction and have been well documented [57, 70-75]. Some of these adverse effects, due to the presence of DC offset current include:

- saturation of the transformer core leading to generation of harmonics
- increase in magnetising current (inductive current) and an increase in VAR absorption
- overheating of the transformer due to current harmonics and skin effects
- increase in acoustic noise emission
- acceleration of corrosive effects

The purpose of this section is to establish that the presence of DC offset current on the secondary side of a power transformer will result in higher levels of harmonic distortion. The aim of the findings in this appendix is also to confirm that the use of the DC offset current controller designed in Chapter 8, will be beneficial in PV inverters that use power transformers.

Varying magnitudes of DC offset current were applied to the primary side of a single phase, 1.2 kVA, transformer, suitable for PV applications. The effect of this DC current on the magnetising current, the primary and secondary voltages and currents was determined. In PV applications, the distortion of the primary voltage due to the DC component of secondary current may be of concern, because the primary is often the point of common coupling for other equipment.

2.0. Application of DC Offset Current

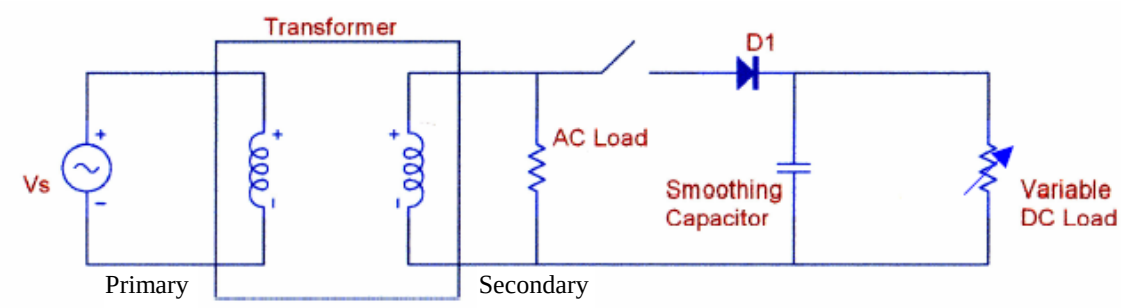

Figure B1: Transformer primary magnetising current with zero DC offset current

The injection of a DC current was achieved by using a half wave rectifier as shown in Figure B1. The transformer was operated under no load conditions and the magnetising current is recorded for different levels of DC offset current.

The first step carried out was to apply up to 200mA (6.67% of rated secondary current) of DC current to the secondary. As expected, the measured value of the DC component of primary current remained zero irrespective of the DC current in the secondary.

The results depicting the effect of DC currents on the secondary magnetising current are shown in Figures B2 and B3. When the DC current in the secondary was zero, the duration of the positive and negation half cycles are 10 ms. This is expected because the

supply frequency is 50 Hz. However, when a positive bias of 80 mA of DC current is present, the duration of the negative half cycle is reduced to 7.5 ms. The magnitude of the negative peak increases to 80 mA. Since no DC current is transferred to the primary, the secondary flux current must also become positive biased. To maintain symmetry, the area encompassed by the positive and negative half cycle of the magnetising current waveform must be equal. Hence, the negative cycle peak increases to compensate for the reduction in the duration of the negative cycle.

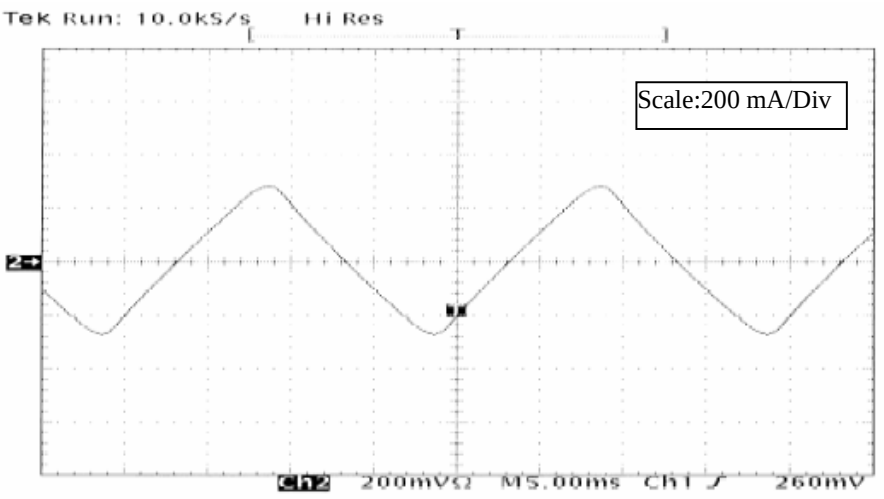

Figure B2: Primary magnetising current with zero DC offset current

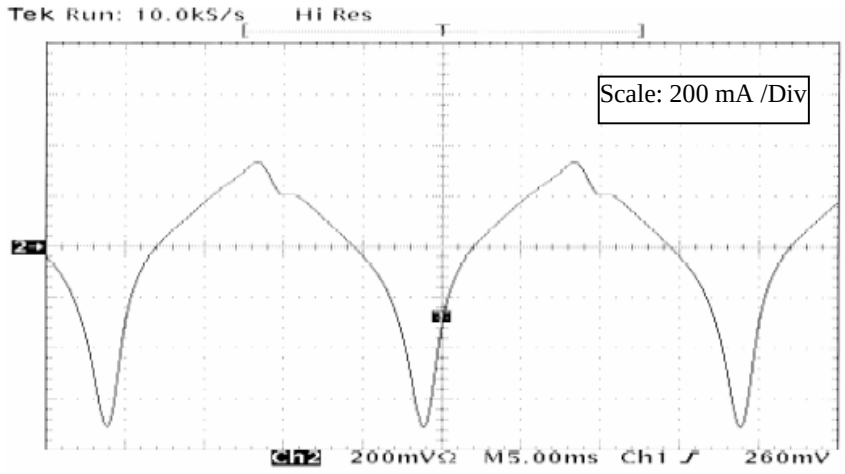

Figure B3: Primary magnetising current with 80 mA DC offset current

In the second part of the test the transformer was operating at its rated output. The level of DC offset current is gradually increased and the distortion of the secondary voltage waveform is illustrated by Figures B4 and B5. The distortion of the secondary voltage will in turn give rise to distortion of the secondary current. A summary of the harmonic components of the secondary voltage is displayed in Figure B6.

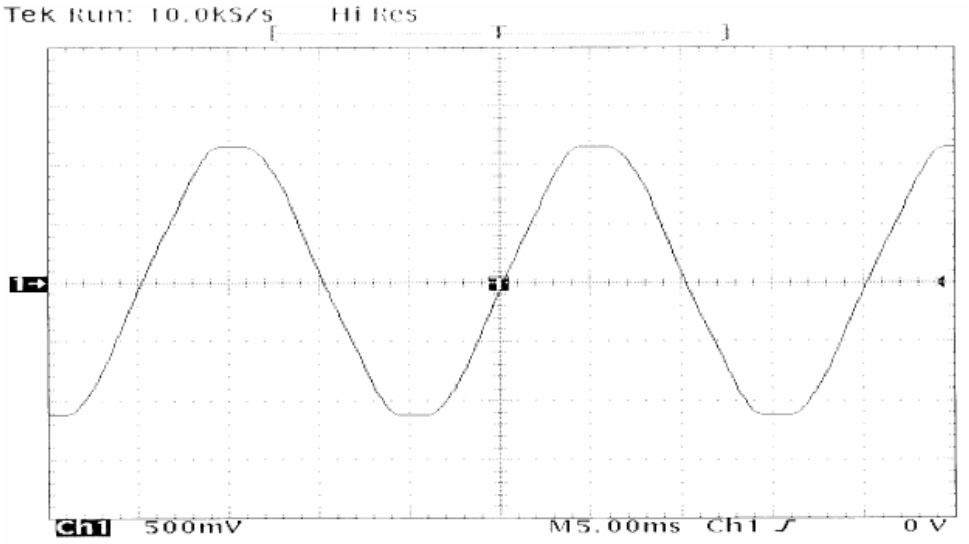

Figure B4: Secondary voltage with zero DC offset current

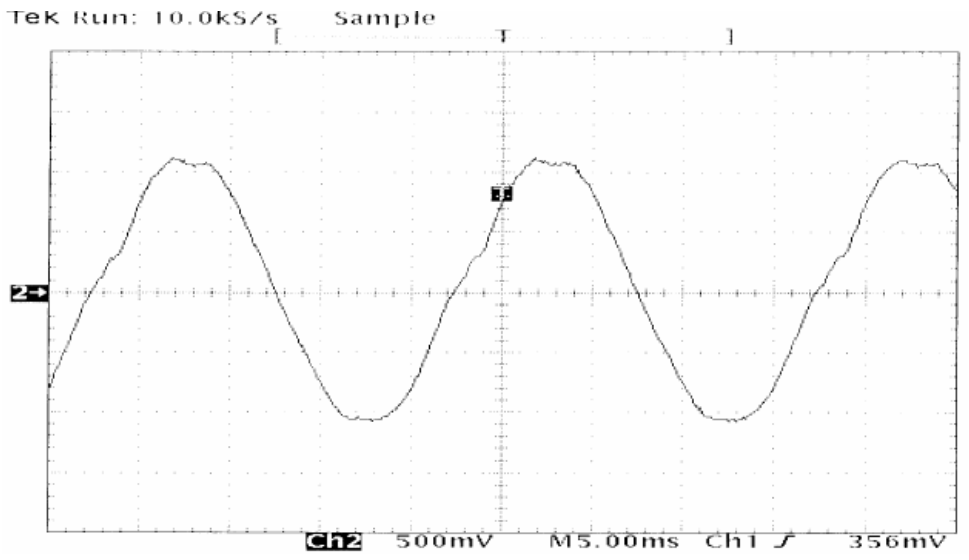

Figure B5: Secondary voltage with 210 mA DC offset current

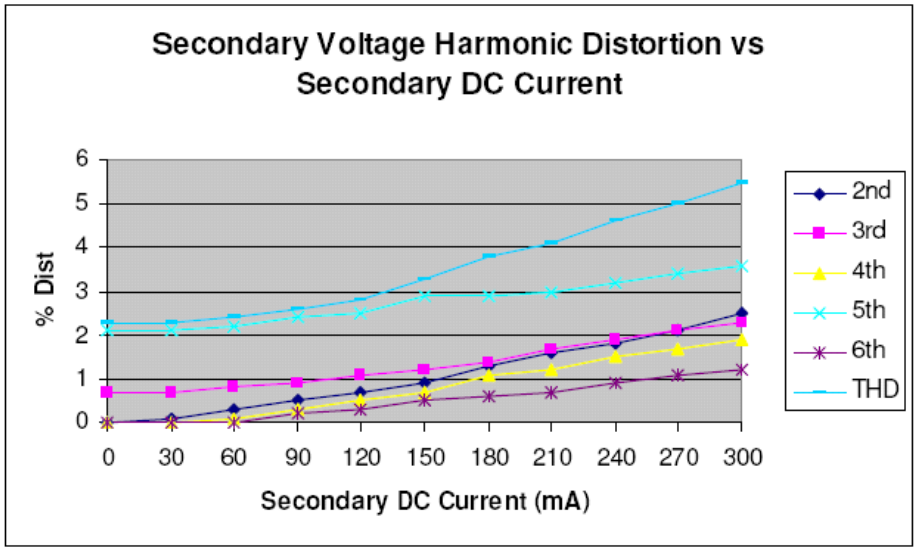

Figure B6: Secondary voltage harmonics due to secondary DC Offset current

The increase in the level of low frequency harmonic components of the secondary voltage, due to the presence of DC offset, is significant. The total harmonic distortion (THD) doubles, from about 2% to about 4% when the DC offset current is increased from

0 A to 0.21 A. The increase in the lower order harmonics is significant, particularly the even harmonics (second and forth). In the next subsection, the impact of the increase in the secondary current harmonics on the primary voltage will be investigated.

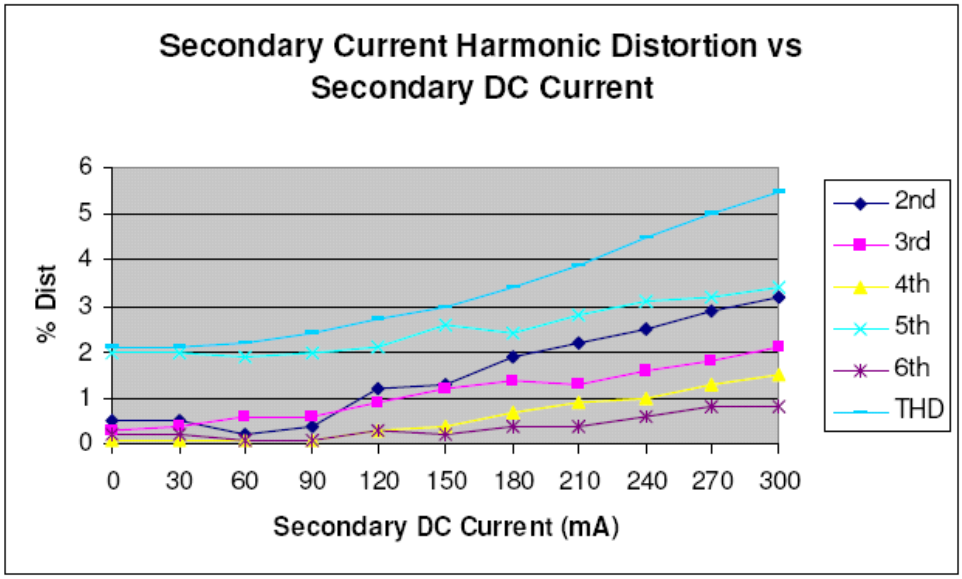

Figure B7: Secondary current harmonics due to secondary DC offset current

3.0. DC Offset Current on Primary Voltage

The distortion of the primary voltage and current, due to the secondary DC current is presented in Figures B8 and B9. The THD of the primary current increased significantly, from about 2% to 11.5% when the secondary DC current was increased from zero to 0.21 A.

The DC offset current of 84 mA measured in Chapter 7, would translate to an increase of about 2% in the third harmonic component of the secondary current, if the same transformer is used.

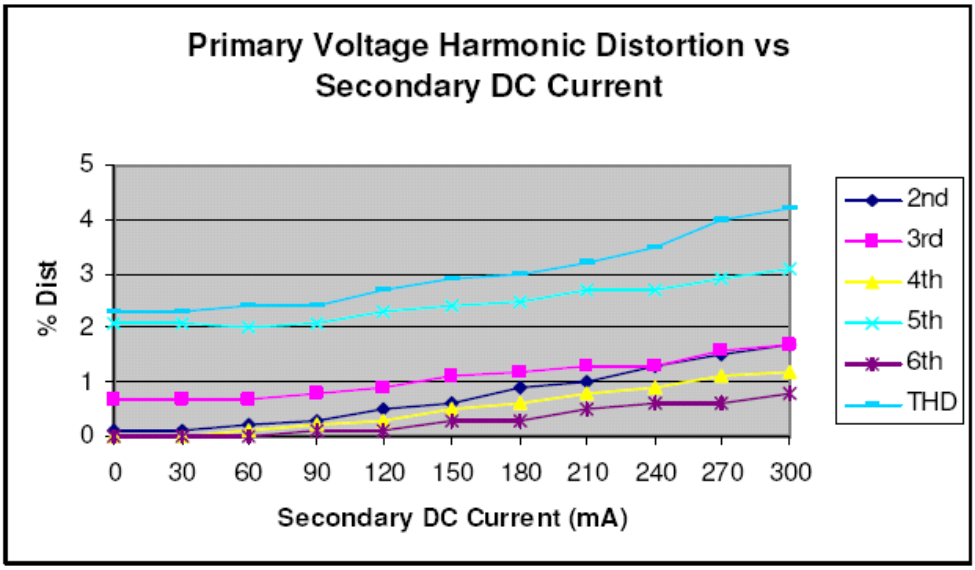

Figure B8: Primary voltage harmonics due to secondary DC offset current

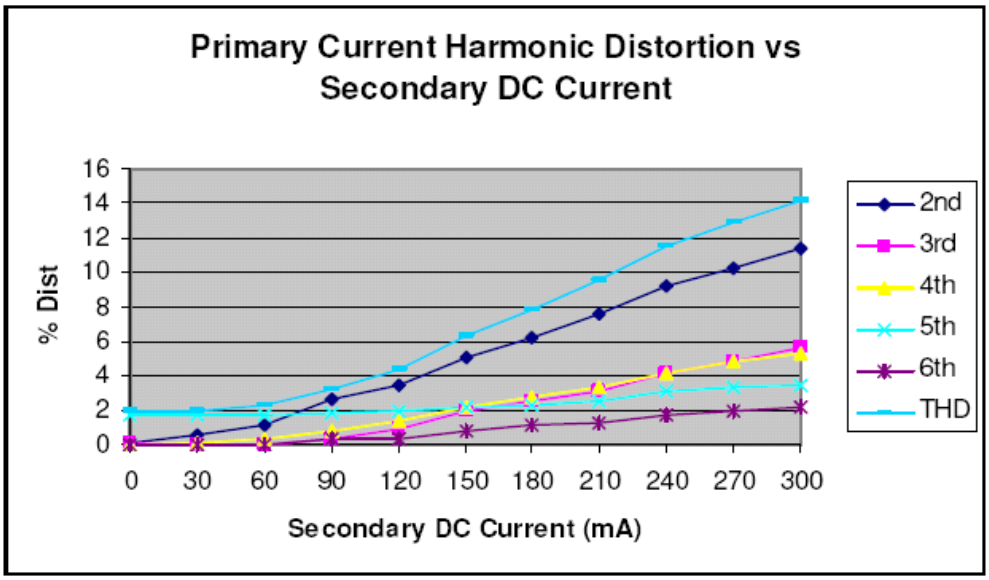

Figure B9: Primary current harmonics due to secondary DC offset current

4.0. Conclusions

The use of power transformers in PV inverters prevents the injection of DC offset currents into the grid system. However, the results presented in this appendix shows that the presence of DC offset currents in the secondary of power transformers, are a source of current and voltage harmonics. In a distributed PV system, these harmonics currents may be a problem to the supply authorities. Therefore, even if transformers are used with grid connected PV inverters, it is an advantage to use minimise these harmonics.

The use of the DC offset current controller designed in Chapter 8, to minimise these harmonics generated by PV inverters that use transformers, is a cost effective and an efficient method. Eliminating the generation of current harmonics at its source, in this case at the inverter output, is the best solution.

APPENDIX C

MODIFIED HYSTERETIC CURRENT CONTROL

1.0. Introduction

Chapter 9 states that the aims of this project have been achieved. Attempts to further improve unipolar switched inverters are therefore outside the scope of this project. This appendix presents an extension of the idea to reduce low frequency harmonics that was suggested in section 9.4 (Chapter 9).

2.0. Modified Hysteretic Current Control

The output current from a unipolar switched inverter using the traditional hysteretic current control strategy is shown in Figure C.1. The inadequate switching shown in Figure C.1 contributes to the generation of low frequency current harmonics and the reasons for this harmonic problem were explained in subsection 3.10.1 (Chapter 3). To overcome the low switching frequency problem near the current zero crossing, the traditional hysteretic current control must be modified. Adding maximum turn-on and turn-off times to the tolerance band limits, to control the switching frequency of the inverter switches, will be investigated. The aim of this work is to continue to use hysteretic current control for most of the current cycle, and to limit the turn-on and turn-off duration of the inverter switches near the zero crossing.

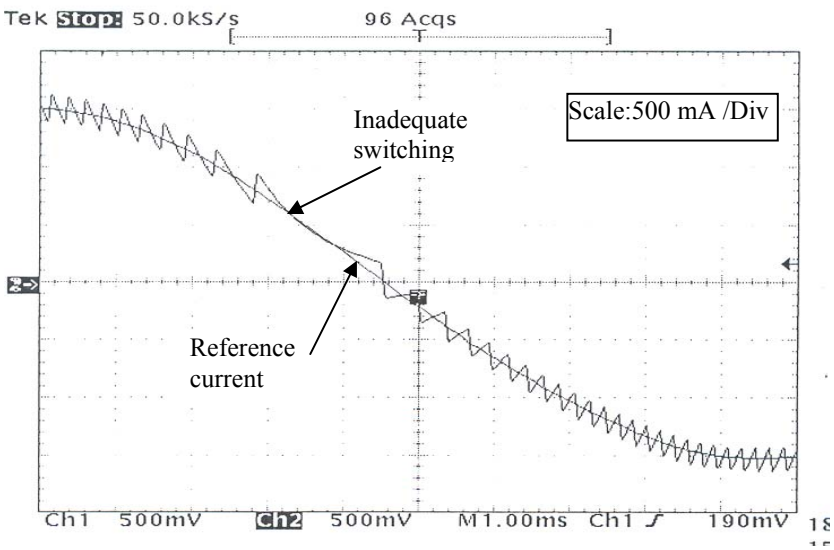

Figure C.1: Hysteretic current control

3.0. Preliminary Experimental Results

A preliminary attempt to use this modified hysteretic current control switching strategy is illustrated in Figure C.2. This test result was obtained when the inverter was supplying a resistive load, and was not connected to the mains supply.

The problem with this initial result was that the turn-on and turn-off periods are not equal. Therefore the average of the inverter output current near the zero crossing will not be equal to the reference current in this region. The minimum frequency generated by the inverter will not be very much different from that shown in figure 3.22(b) in Chapter 3.

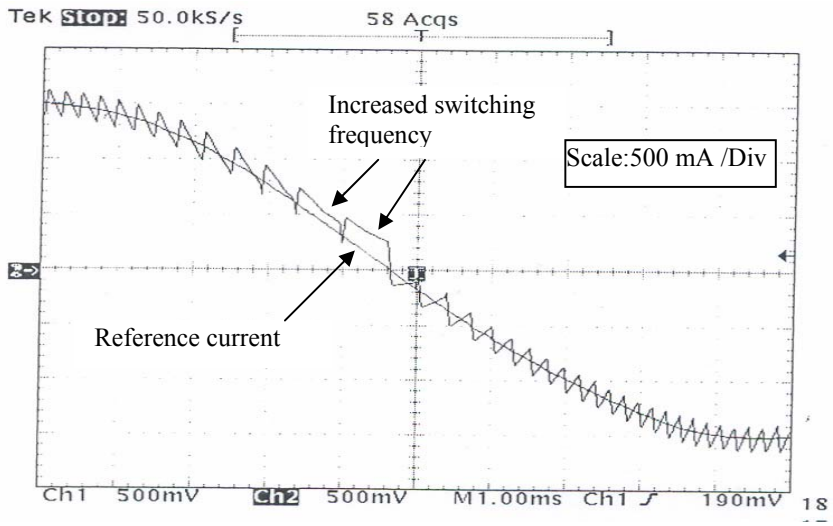

Figure C.2: Modified hysteretic current control

To demonstrate the preferred equal turn-on and turn-off periods of the inverter switches, the magnitude of the reference current was reduced to less than that of the magnitude of the tolerance band 0.2A. Since the reference current remains within the tolerance band and does not cross the upper or lower limits, switching should occur only at the zero crossing, if the traditional hysteretic current control is used (Figure C.3).

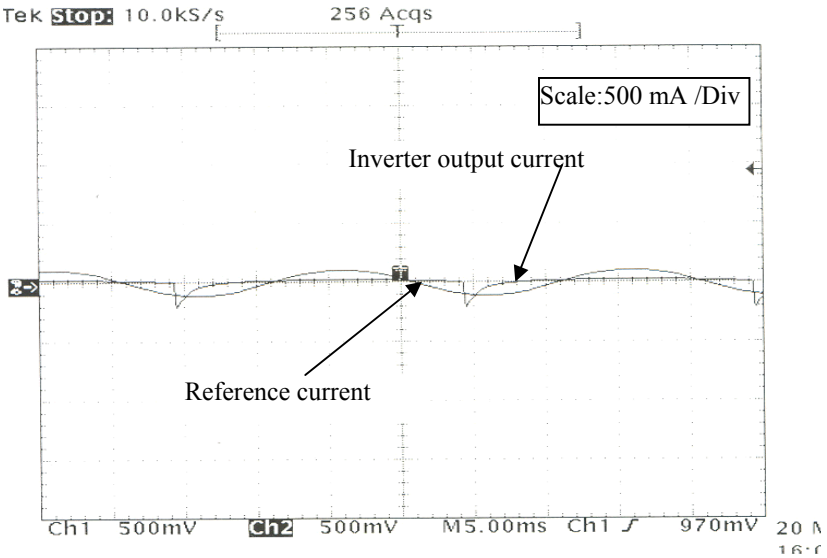

Figure C.3 Hysteretic current control with $I_s \leq I_{Tol}$

If on the other hand, a maximum time limit is applied to the turn-on and turn-off periods of the inverter switches, then the switching frequency will be as shown by Figure C.4. If this concept can be successfully applied to an inverter supplying currents up to its rated value then it should be possible to reduce the low frequency harmonics generated by a (modified) hysteretic current control inverter.

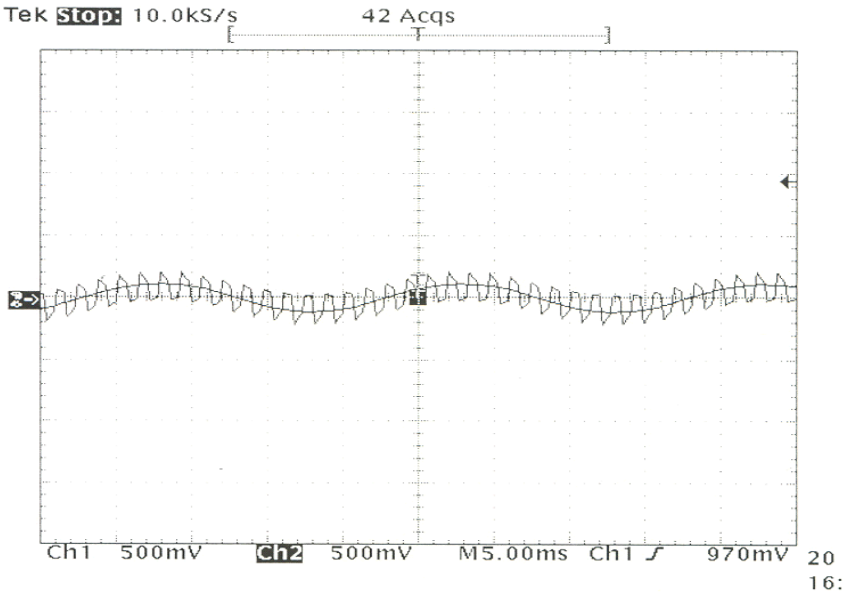

Figure C.4: Modified CCL test results

4.0. Conclusions

It has been demonstrated that controlling the maximum turn on and turn off period of the inverter switches to increase the minimum switching frequency is possible. However, a lot more work needs to be done before the modified hysteretic current control technique can be tested with utility connected PV inverters. The implementation of this control technique also needs to be cost effective.

APPENDIX D

INVERTER GATE DRIVE CIRCUITS

1.0. Circuit Layout

The circuit diagram for each of the four gate drives for the inverter bridge is the same as the circuit shown in Figure A1 (Appendix A). The current controller provides signals to gate drive circuits at the appropriate time, to turn on or turn off the correct IGBTs switches T_{A+}, T_{A-}, T_{B+}, and T_{B-} shown in Figure 3.1 (Chapter3).

The printed circuit board layout and the final circuit constructed for the gate drives are shown in Figures D1 and D2 respectively.

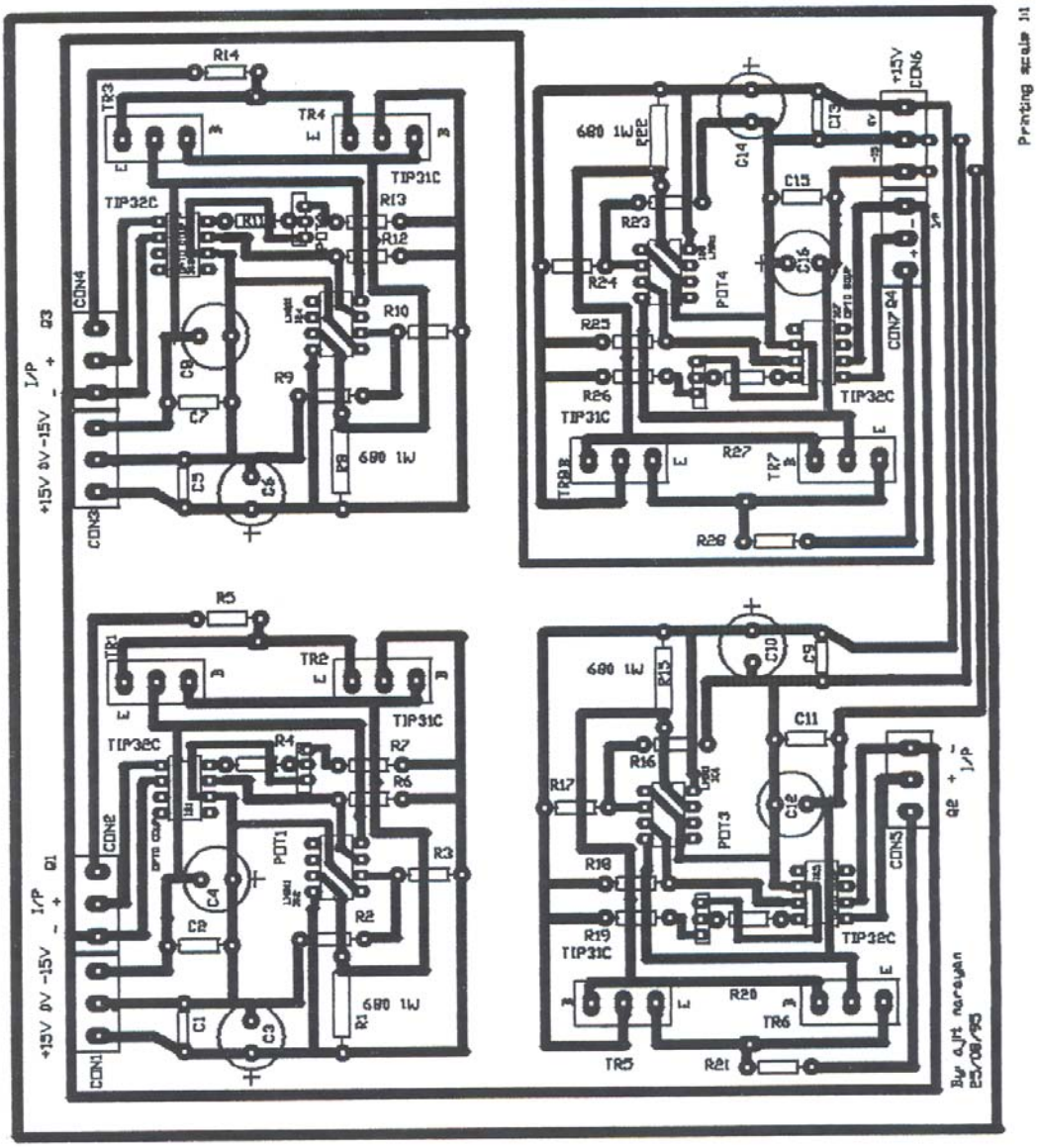

Figure D1: Schematic PCB artwork for four gate drives

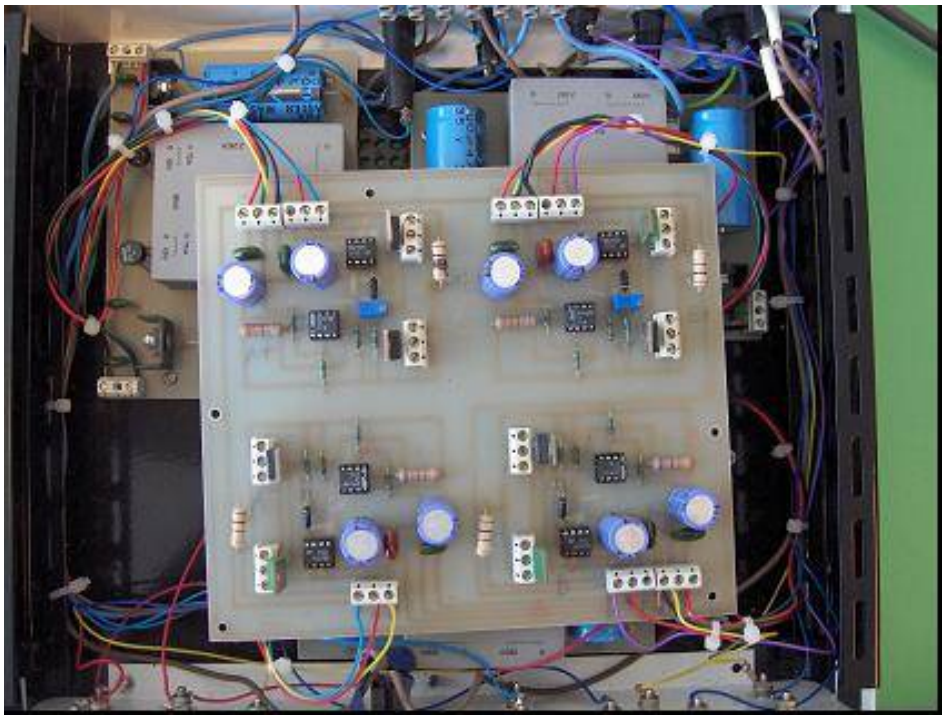

Figure D2: Four gate drives for Inverter Bridge.

APPENDIX E

ADDITIONAL EXPERIMENTAL RESULTS

1.0. Introduction

The 1kW PV panels used to test design procedure of the inverter system are shown in Figure E1. While only essential results to validate the design procedure are included in the main text, additional experimental results using the PV panels in Figure E1 have been included in Appendix E to show the following:-

- the importance of setting the DC voltage reference correctly
- the inverter operating at unity power factor
- the inverter operation at low current levels.
- the effects of delay on the performance of the inverter

Figure E1: 1 kW BP Model 275, PV system used for testing inverter control loops.

2.0. DC reference voltage

It has been explained in Chapter 2 that the function of the voltage control loop is to keep the input DC voltage V_c constant. To be able to achieve this condition, the value chosen for the DC reference voltage V_{ref} (Figure 3.1) is important. The ratio of the peak value supply voltage V_s (set by the supply authorities) to V_c will be influenced the performance of the inverter. For example, if the ratio of V_s/V_c is 93% then distortion of the current will occur as shown in Figure E2. Keeping all the inverter parameters unchanged except reducing the ratio of V_s/V_c to 86% is shown in Figure E3. The reduction of the ratio eliminates the current distortion problems. This problem could have also been solved by reducing delay.

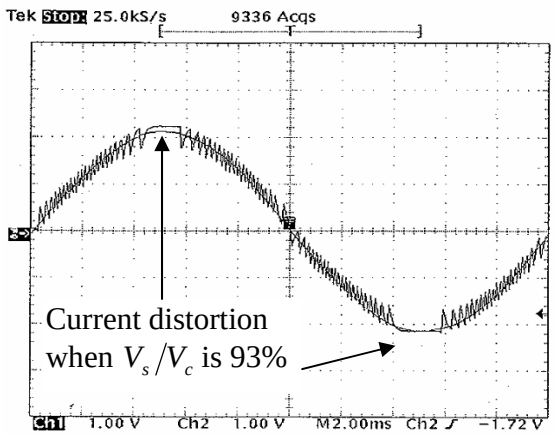

Figure E2: Distortion of inverter output current when V_s/V_c is 93% (i_s = 1.5 A)

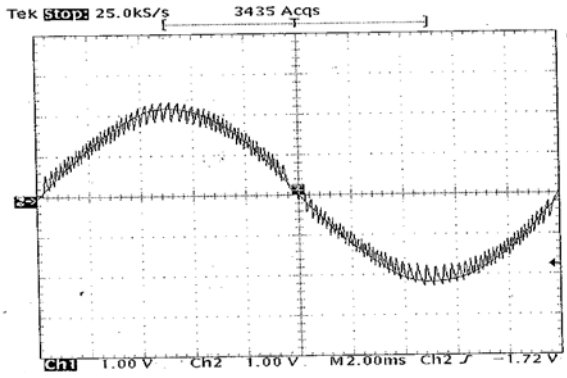

Figure E3: Distortion free inverter output current when V_s/V_c is 86% (i_s = 1.5 A)

The above results demonstrate the significance of choosing value of V_{ref} and hence V_c correctly.

3.0 Inverter Power Factor

The output voltage V_{fs} from zero phase shift filter B in Figure 3.1 (Chapter 3) is shown in Figure 7.3 in Chapter 7. The function of the current controller is to force the inverter output to follow the sinusoidal reference voltage. Therefore the inverter operates at unity power factor.

The experimental results shown in Figures 5.20, 5.22 (Chapter 5), is an example of the inverter injecting a current of 2.2 A into the grid system at almost unity power factor. However, a better illustration of the inverter operating at unity power factor is shown in Figures E3 and E4. In these cases it show that varying the current injected into the grid from 1.5 A to 0.7 A does not have any effect on the power factor of the inverter system.

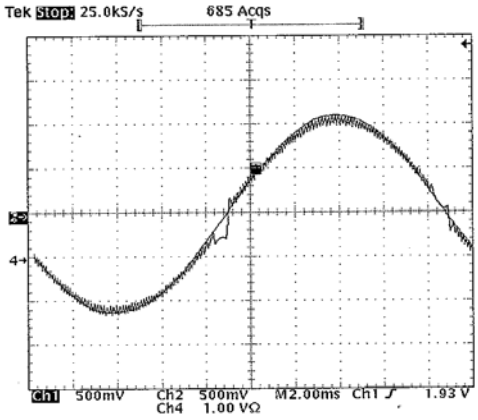

Figure E4: Inverter operating at unity power factor (i_s = 0.7 A)

4.0. Current Distortion due to Switching Delay

Switching delay was minimized to obtain the results presented in Figure 5.20 (Chapter 5). The results in Figures E5 and E6 are presented to demonstrate the impact of switching delay on the quality of the inverter output current. It further illustrates that switching delay cannot be ignored when designing inverters.

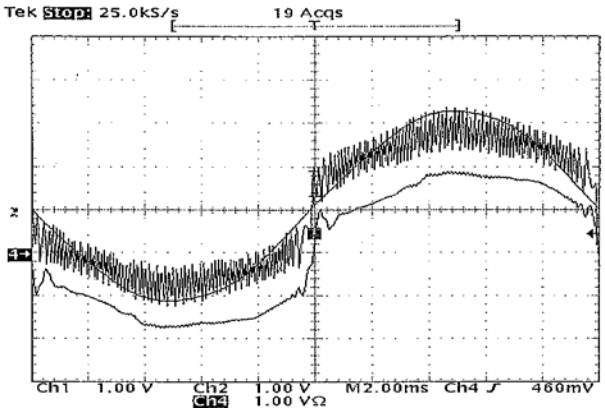

Figure E5: Current Distortion when Inverter switching delay is 16µs

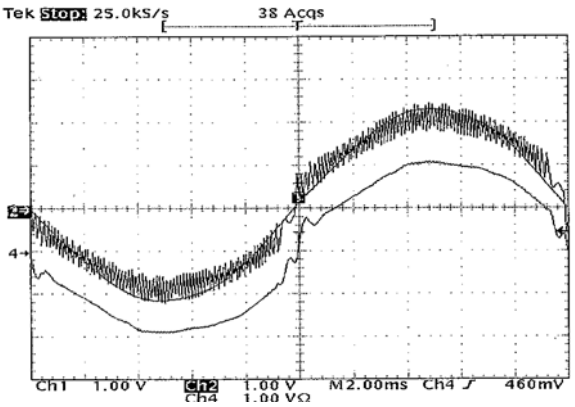

Figure E6: Current Distortion when Inverter switching delay is 6µs