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Orientation dependence of the pseudo-Hall effect in p-type 3C–SiC four-terminal devices under mechanical stress†

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This paper presents for the first time the orientation dependence of the pseudo-Hall effect in p-type 3C–SiC four-terminal devices under mechanical stress. Experimental results indicate that the offset voltage of p-type 3C–SiC four-terminal devices significantly depends on the directions of the applied current and stress. We also calculated the piezoresistive coefficients π_{61}, π_{62}, and π_{66}, showing that π_{66} with its maximum value of approximately 16.7×10^{-11} Pa^{-1} plays a more dominant role than π_{61} and π_{62}. The magnitude of the offset voltage in arbitrary orientation under stress was estimated based on these coefficients. The finding in this study plays an important role in the optimization of Microelectromechanical Systems (MEMS) mechanical sensors utilizing the pseudo-Hall effect in p-type 3C–SiC.

Silicon Carbide (SiC), with its large energy band gap (2.3–3.4 eV) and superior mechanical properties, is an excellent candidate for electrical devices operating in harsh environments.[1–5] Recent studies have paid significant attention to the characterization of the strain effect on SiC for sensing applications under hostile conditions.[6–8] Many groups have reported the piezoresistive effect in various poly types of SiC such as 3C–SiC, 4H–SiC, and 6H–SiC. Large gauge factors of approximately 30 were reported in both p-type and n-type single crystalline SiC, indicating that SiC has high potential for mechanical sensing applications.[9–14] Among more than 200 poly types of crystalline SiC, cubic crystalline silicon carbide (3C–SiC) is preferable for Microelectromechanical systems (MEMS) transducers. The main advantage of 3C–SiC over other poly types is the capability of growth on a silicon (Si) substrate, which reduces the cost of wafers and is more compatible with the conventional MEMS process.[2,12–15] Most previous studies on the piezoresistive effect of SiC utilized the conventional two-terminal resistors requiring

a Wheatstone bridge for voltage read-out,[15,16] which faces several drawbacks. For instance, the four resistors in the bridge must be closely identical to obtain a zero offset.[17–19] In addition, the resistors in the Wheatstone bridge must have almost the same temperature coefficient to avoid the offset drift due to the change of temperature.[20] Compared to two-terminal resistors, four-terminal devices have proved to be more thermally stable and suitable for the miniaturization of sensors, since they do not require any external Wheatstone bridge.[17–21] Under a mechanical shear strain, a voltage is generated across two terminals of four-terminal devices due to the distortion of potential distribution, and this phenomenon has been named as the pseudo-Hall effect.[22,23] To date, there have been various studies on the pseudo-Hall effect in silicon material, and in fact this effect in Si has been utilized in commercial strain sensors for more than two decades.[23,24] However, the work on the pseudo-Hall effect in SiC has been rarely reported.[25] As the pseudo-Hall effect in semiconductors depends on the crystallography orientation, it is important to investigate which orientation offers the most significant effect in 3C–SiC four-terminal devices.

In this paper, we report on the orientation dependence of the pseudo-Hall effect in p-type 3C–SiC thin films. The piezoresistive coefficients, π_{61}, π_{62}, and π_{66}, which define the magnitude of the pseudo-Hall effect were also investigated. The insight gained in this study is vital to the development of MEMS mechanical sensors using the pseudo-Hall effect in 3C–SiC.

The 3C–SiC thin films were grown on (100) Si substrate using low pressure chemical vapor deposition (LPCVD)[26] at a low temperature of 1000 °C. The alternating supply epitaxy approach was used to achieve single crystalline SiC film deposition with silane (SiH$_4$) and propylene (C$_3$H$_6$) as precursors. Aluminum was employed as the dopant in the *in situ* doping process where trimethylaluminum [(CH$_3$)$_3$Al, TMAl] was the precursor to form p-type 3C–SiC. The properties of the grown single crystalline 3C–SiC films were characterized and reported elsewhere.[26,27] The X-ray diffraction (XRD) measurement indicated that the SiC film is epitaxially grown on Si (100) substrate,

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Fig. 1(a). Based on the X-ray photoelectron spectroscopy data, the atomic concentrations of carbon and silicon were found to be approximately 52.9% and 47.1%, respectively, while that of aluminum was below 1%. The atomic force microscopy (AFM) image of a 380 nm 3C–SiC film shows that the roughness of a 5 μm × 5 μm area was 20 nm, Fig. 1(b). The semiconductor type and carrier concentration of the films were then investigated using the hot probe method.[28] The positive voltage at the hot probe indicated the 3C–SiC film was p-type semiconductor, and the carrier concentration was calculated to be in the range of 10^{18} cm^{-3}. Fig. 1(c) shows the fabrication of the 3C– SiC four-terminal device using a 2-masks-photolithography process. In the first step, SiC pattern was formed using Inductively Coupled Plasma (ICP) etching with an etch-rate of approximately 200 nm min^{-1}.[27] Next, aluminum was deposited on the SiC film using sputtering, and aluminum electrodes were then patterned using wet etching. Finally, the SiC/Si wafers were diced into smaller strips with dimensions of 9 mm × 60 mm × 0.6 mm for the subsequent bending experiment, Fig. 1(d). A photograph of the fabricated devices and a schematic sketch of the current and applied stress are shown in Fig. 1(e) and (f).

The linear current–voltage characteristics of the SiC four-terminal devices were measured using ™HP4145B, indicating a good Ohmic contact between the aluminum electrodes and the p-type 3C–SiC films. The current leakage between the 3C–SiC layer and the Si substrate was also investigated to ensure

that Si substrate did not contribute to the measured results (see the ESI†). To characterize the pseudo-Hall effect in the four-terminal SiC devices, we applied stress to the SiC films using the bending beam method, while supplying a constant current through terminals 1 and 2 and monitoring the change of the generated voltage across terminal 3 and 4 of the SiC devices, Fig. 1(d) and (f). Since the thickness of the SiC films (~300 nm) is less than 0.1% of that of the Si substrate (600 μm), we assumed that the strain induced into the SiC films is approximately equal to that of the surface of the Si substrate: $\varepsilon = Mt/2E_{Si}I$, where M is the bending moment; I is the moment of inertia; E_{Si} and t are the Young's modulus and the thickness of the Si layer, respectively. Accordingly, for an applied load varied from 0 to 2 N to the free end of the Si strips, the strain induced into the SiC layer was in a range of 0 to 900 ppm. The stress applied to the SiC layer (σ_{SiC}) was then calculated using Hooke's law: $\sigma_{SiC} = E_{SiC}\varepsilon$, where E_{SiC} is the Young's modulus of 3C–SiC.[29]

We investigated the orientation dependence of the pseudo-Hall effect of p-type 3C–SiC thin films by characterizing SiC four-terminal devices aligned in different directions and being stressed in different orientations, as summarized in Table 1. Fig. 2 shows that for sample A (the orientation of the current is [100], and the direction of the stress is [110]), an offset voltage was generated across terminals 3 and 4 when we applied a stress in [110] orientation. It is also clear that, the offset voltage increased when increasing the applied stress to 264 MPa. The offset voltage then decreased with decreasing the stress, and returned to 0 when the load was completely removed. The generated voltage of the SiC four-terminal resistors under stress was measured for several testing cycles, showing a good reproducibility without any significant drift voltage (see ESI†). This indicates the feasibility of using the pseudo-Hall effect in p-type 3C–SiC four-terminal devices for MEMS strain/stress sensors.

The same phenomenon was also observed in other samples (B, C, D, E, F), but with different order of magnitude. Fig. 3 shows the ratio of the output voltage to the input voltages of different samples A, B, C, D, E and F, indicating a linear relationship between the output offset voltage (V_{out}/V_{in}) and applied stress (σ). These results also show that the magnitude of the generated offset voltage in 3C–SiC four-terminal devices varies with the directions of the current and the applied stress, indicating the orientation dependence of the pseudo-Hall effect in
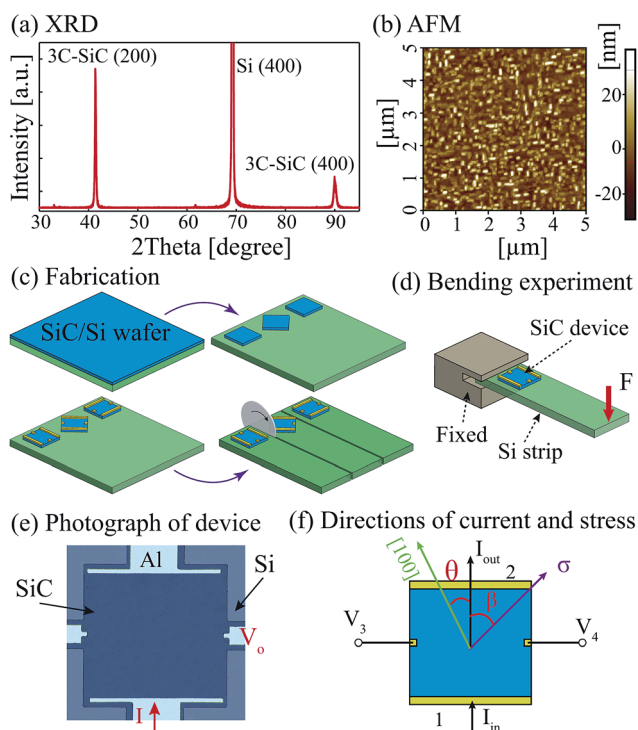

Fig. 1 (a) The XRD graph of the 3C−SiC film grown using the LPCVD process; (b) the AFM image of a 380 nm SiC film; (c) the fabrication process; (d) the bending experimental setup; (e) the photograph of a SiC four-terminal device with its dimensions of 500 μm × 500 μm; (f) schematic sketch of the directions of the current, voltage and applied stress.

Table 1 List of SiC four-terminal samples[a]

Test samples	Orientation of current	Orientation of uniaxial stress	θ	β
A	[100]	[110]	0°	45°
B	[110]	[110]	45°	0°
C	[110]	[1$\bar{1}$0]	45°	90°
D	[110]	[100]	45°	45°
E	[100]	[100]	0°	0°
F	[100]	[010]	0°	90°

[a] θ is the angle between the direction of the applied current and [100] orientation, and β is the angle between the directions of the applied stress and the current in 3C–SiC (100) plane.
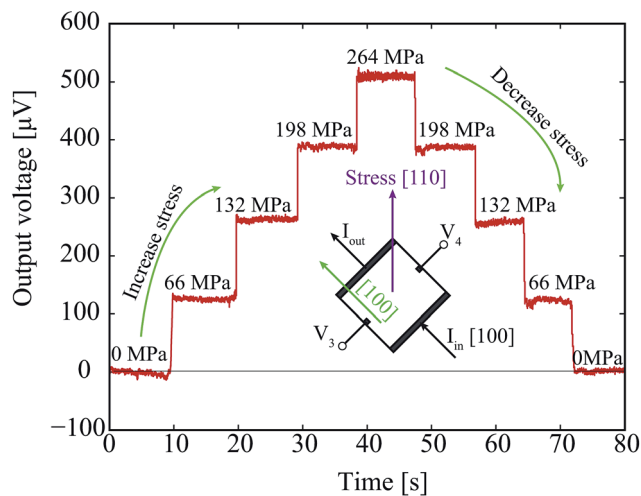
Fig. 2 The generated voltage across terminals 3 and 4 when supplying a constant current of 10 μA through terminals 1 and 2 of a SiC four-terminal devices under several applied stresses from 0 to 264 MPa. Note that the orientation of the current is [100], while that of the applied stress is [110] in (100) plane.

p-type 3C–SiC thin film. As 3C–SiC has the cubic crystalline structure like Si, we qualitatively and quantitatively explained the pseudo-Hall effect and its orientation dependence in p-type 3C–SiC, using the model proposed by Kanda *et al.* for the case of Si.[17,30] Fig. 3 (inset) shows an equivalent circuit of the four-terminal device, which consists of four resistors R_{13}, R_{14}, R_{23}, and R_{24}. In the strain-free state, these four resistors are considered to be identical ($R_{13} = R_{14} = R_{23} = R_{24}$). Under a uniaxial mechanical strain as shown in Fig. 1(d), these four resistors are stressed, and their resistances change. As R_{13}, R_{14}, R_{23}, and R_{24} are aligned in different orientations, these resistance changes are different, leading to an unbalance of the bridge circuit, which results in a non-zero voltage across terminals 3 and 4. The ratio of the generated voltage (V_{out}) across terminals 3 and 4 to the applied voltage across terminals 1 and 2 (V_{in}) due to stress can be quantified by the coefficients π_{61}, π_{62}, and π_{66}, as expressed in the following equation (see the ESI†)[33,34]:

$$V_{out} = V_{in} (\pi_{61}\sigma_1 + \pi_{62}\sigma_2 + \pi_{66}\sigma_6) \qquad (1)$$

where σ_1 and σ_2 are normal stresses parallel and perpendicular to the current, and σ_6 is the in-plane shear stress which are calculated from the applied uniaxial stress σ, using Mohr's circle (see the ESI†):

$$\begin{cases} \sigma_1 = \sigma \cos^2 \beta \\ \sigma_2 = \sigma \sin^2 \beta \\ \sigma_6 = -\dfrac{\sin 2\beta}{2}\sigma \end{cases} \qquad (2)$$

here, β is the angle between the applied uniaxial stress (σ) and the current. The piezoresistive coefficients are defined in the following equation[30,31] (see the ESI†):

$$\begin{cases} \pi_{61} = -\dfrac{1}{4}a \sin 4\theta \\ \pi_{62} = \dfrac{1}{4}a \sin 4\theta \\ \pi_{66} = b + a \sin^2 2\theta \end{cases} \qquad (3)$$

where θ is the angle between the direction of the applied current and [100] orientation in (100) plane, and $a = \pi_{11} - \pi_{12} - \pi_{44}$ and $b = \pi_{44}$ are constant parameters. Thus, by measuring the change of the generated voltage in samples A and D, we can determine parameters a and b, and consequently, the piezoresistive coefficients π_{61}, π_{62} and π_{66}. From the experimental results shown in Fig. 3, a and b were calculated to be -14.8×10^{-11} Pa^{-1} and 16.7×10^{-11} Pa^{-1}, respectively. As a result, substituting a and b into eqn (3), the magnitude of the coefficients in any arbitrary orientation on (100) plane can be estimated, Fig. 4. These results show that for the p-type 3C–SiC four-terminal devices, the coefficient π_{66} plays a more dominant role than π_{61} and π_{62}. The experimental data obtained in samples B, C, E, F was also in good agreement with the theoretical calculation that the output offset voltage was approximately 0, since the coefficients π_{61} and π_{62} are 0 when θ is equal to 0 or $\pi/4$ radian.

Based on the coefficients, we estimated the magnitude of the output offset voltage of 3C–SiC four-terminal devices under stress for MEMS mechanical sensors. Substituting eqn (2) into eqn (1), and using the calculated piezoresistive coefficients shown in Fig. 4, it is possible to theoretically estimate the magnitude of the pseudo-Hall effect of 3C–SiC four-terminal devices aligned in arbitrary orientations. Fig. 5 shows the ratio of the generated voltage to the applied voltage per unit applied stress ($[V_{out}/V_{in}]/\sigma$). It is obvious that, the magnitude of the effect in p-type 3C–SiC varies with orientations of current and stress. Accordingly, in (100) plane, the absolute offset voltage ($|V_{out}|$) gains its maximum value when $(\theta, \beta) = (m\pi/2, (2n + 1)\pi/4)$, where m and n are integers. Therefore, when
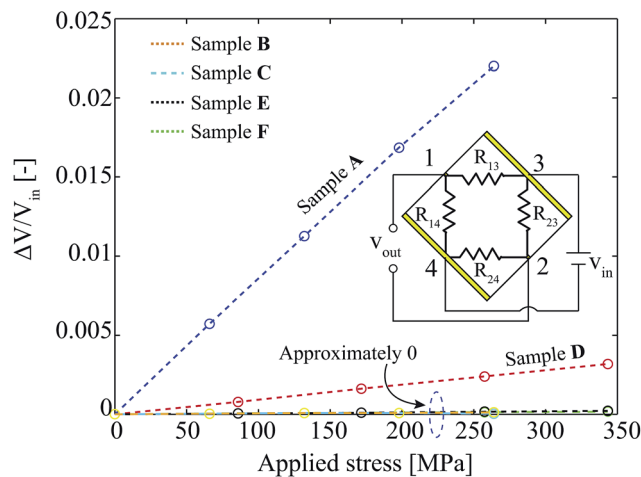

Fig. 3 The ratio of the generated voltage and applied voltage of the SiC four-terminal devices aligned in different orientation. Inset: the equivalent four resistors R_{13}, R_{14}, R_{23}, and R_{24} of a 3C–SiC four-terminal device.[32]
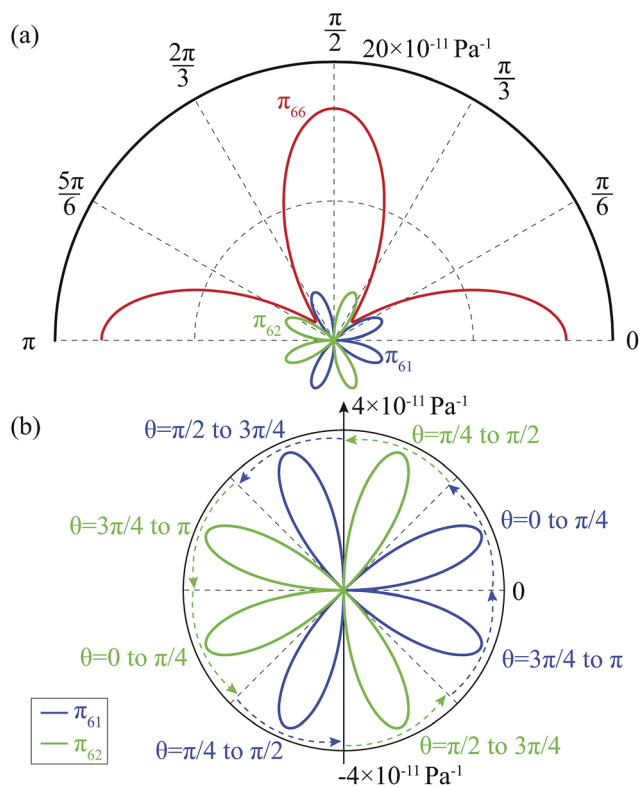
Fig. 4 (a) The coefficients π_{61}, π_{62}, and π_{66} of SiC four-terminal devices when θ varies from 0 to π; (b) π_{61} and π_{62} are plotted in a different scale.

designing MEMS mechanical sensors using the pseudo-Hall effect in p-type 3C–SiC four-terminal resistor, these orientations should be chosen to enhance the sensitivity of sensors. On the other hand, for the Hall-devices where a constant offset voltage under external stress is desired, the orientations of (θ, β) = $(m\pi/4, n\pi/2)$ should be selected to minimize the pseudo-Hall effect (here m and n are integers).

In conclusion, we reported on the pseudo-Hall effect in p-type 3C–SiC four-terminal devices, the orientation
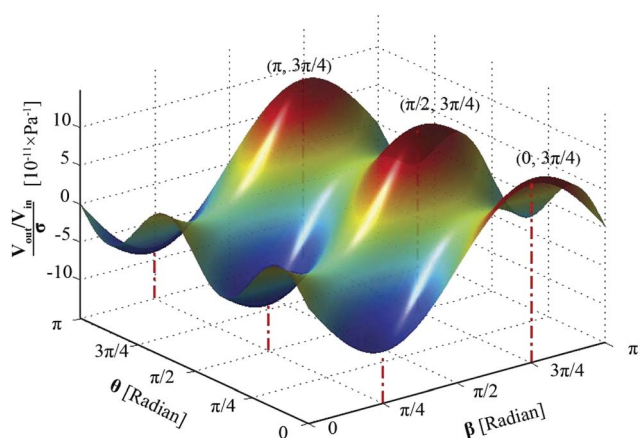
dependence, and piezoresistive coefficients π_{61}, π_{62}, and π_{66}. The maximum value of π_{66} was found to be 16.7×10^{-11} Pa^{-1}, while that of π_{61} and π_{62} was 3.7×10^{-11} Pa^{-1}, implying that π_{66} plays a more dominant role than the other coefficients. Based on these piezoresistive coefficients, it is possible to estimate the magnitude of the pseudo-Hall effect in any arbitrary orientation. Furthermore, the large output voltage at a certain applied current and stress along with a direct/simple signal-readout method indicate that pseudo-Hall effect in p-type 3C–SiC is a good candidate for MEMS applications. These findings in this study play an important role in designing/optimizing MEMS mechanical sensors as well as Hall devices utilizing p-type 3C–SiC material.

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Fig. 5 The ratio of the generated voltage across terminals 3 and 4 to the input voltage across terminals 1 and 2 per unit uniaxial stress σ.

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