REMOVAL OF DC OFFSET CURRENT FROM TRANSFORMERLESS PV INVERTERS CONNECTED TO UTILITY

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ABSTRACT

Some electricity supply authorities in Australia allow PV inverters of up to 10 kW output to be directly connected to their grid network. The benefits of avoiding the use of power transformers in such PV applications are higher conversion efficiency of the PV system and lower costs. These benefits however, can only be realised if the level of DC offset current injected from such transformerless inverter systems is maintained within the stringent limits governed by Australian Standard AS4777.2. Currently, there is a lack of evidence that the level DC offset current can be economically and efficiently maintained within these legal limits. In this paper, it is shown that irrespective of its source, the DC offset current can be maintained within these limits without sacrificing the overall conversion efficiency of the inverter system. Simulation and experimental results are presented to confirm that this simple, cost effective technique can be used to measure and separate small magnitudes of DC offset currents from large values of AC currents without compromising the dynamic response of the current feedback loop. This new technique can also be used to improve the quality of the power supplied by PV inverters that use power transformers.

Keywords: PV Inverters, Transformerless, Unipolar Switched, DC Offset Current.

1. INTRODUCTION

The conversion efficiency of single-phase, PWM, current controlled inverters can be improved by using unipolar switching [1]. Unipolar switching also allows inverter designers the ability to choose one of four equivalent switching combinations to change the polarity of the DC voltage across the output inductor and to force the current to stay within a small tolerance band. The use of only one of these four combinations, however, leads to the elimination of the high frequency electrical noise generated by the switching action, without the need for additional filters [2]. Significant reduction in voltage transitions during switching is also an advantage from the point of view of EMI generation.

The disadvantage of unipolar switched inverters using hysteretic current control is that they generate low frequency harmonics due to switching circuit delay. However, it has been shown that such inverters can still be designed to meet the requirements of Australian Standard AS4777.2 [3].

Current control offers advantages such as active current waveshaping, inherent current limitation and automatic synchronisation with the utility grid [4]. For simplicity and excellent dynamic performance characteristics the current loop may be based on hysteretic control [5]. The disadvantage of hysteretic control is, that the inverter switching frequency varies along the AC current waveform [6]. This varying switching frequency produces current harmonics that may interfere with the operation of other equipment connected to the same local supply. Current control design procedures to estimate the switching frequencies along the current waveform have lead to the design of simple switching frequency filters to minimise these current harmonics [2, 7].

Based on these proven advantages of using unipolar switching and current control, it was decided that a PWM, hysteretic current control, transformerless, unipolar switched inverter be used to develop a new technique to remove DC offset currents from its output.

This paper therefore, aims to establish if the DC offset current injected by transformerless PV inverters into the grid system can be economically and efficiently maintained within the limits specified by Australian Standard AS4777.2.

2. DC OFFSET CURRENT

In Australia, PV inverters can only be directly connected to the grid if the DC offset current injection does not exceed 5 mA or 0.5 % of the rated output current (whichever is greater) [8]. Keeping below these limits will prevent accelerated electrolytic corrosion of the earthing conductors and prevent power distributions transformer that normally operate near saturation, into saturation [9].

The sources that contributed to the DC offset current present in the inverter output included: -

- the impedance of the two arms the inverter-bridge not being perfectly equal;
- DC offset present in the reference current; and
- DC offset current introduced by Hall Effect current sensors.

It has been shown that the small value of resistance of the inverter outer current loop was sufficient to allow the use of a simple RC circuit to provide the necessary level of voltage feedback to the current controller, to reduce the DC offset current [9]. The advantage of this method of measuring the DC voltage (due to the DC offset current) was that it does not introduce additional DC offset current. The disadvantage of the approach used by Masoud and Ledwich [9] was that it failed to provide adequate separation of the DC voltage from the AC voltage despite using an integrating stage after the RC output circuit. However, in this project total attenuation of the ripple voltage was required to prevent unacceptable levels of DC offset current being injected into the grid system.

3. INVERTER SYSTEM

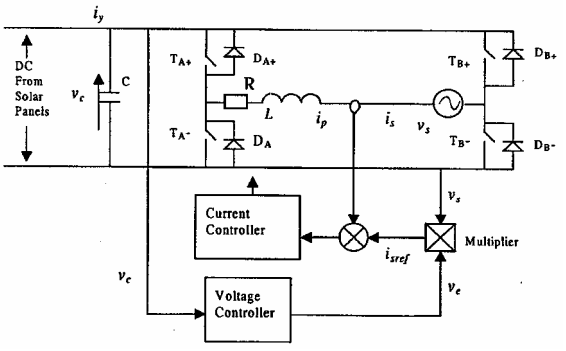

Figure 1: Inverter Voltage and Current Control Loops

The utility connected inverter system being considered, shown in figure 1, has two control loops: the current control loop (CCL) and the voltage control loop (VCL). The function of the VCL is to keep the DC voltage v_c constant [10]. In this paper the VCL is assumed perfect and the 3rd harmonics, due to the 2nd harmonics in V_c, are ignored.

Hysteretic control with a fixed tolerance band, I_{tol}, is used to force current i_p to track the reference sinusoidal current i_{sref}. The controller forces the bridge into one of four possible states depending on the need to make $|i_p|$ rise or fall and on the polarity of v_s. Whenever $|i_p|$ s falling and reaches the bottom current limit, $|i_p|$ - $0.5I_{tol}$, $|i_p|$ is made to rise by switching on T_{A+} and T_{B-} if v_s is positive or T_{B+} and T_{A-} if v_s is negative. Due to circuit component imperfections there is a time delay t_d between the instant $|i_p|$ reaches the bottom current limit and the instant the inverter changes state (Figure 2). Whenever $|i_p|$ reaches the top current limit, $|i_p| + 0.5I_{tol}$, $|i_p|$ is made to fall by turning off one of the previously conducting pair of transistors. Again there is a time delay between the instant $|i_p|$ reaches the top limit and the instant the inverter changes state

Since the supply voltage $\hat{V}_S$, is set by the power supply authorities at 340 V, to minimise distortion, V_c was chosen as 400 V. A 1 kW PV system is being considered, hence, the rated current is used as the value for I_s ($\hat{I}_S$ = 5.9 A and ω = 314 rad/s). Since the inductance of the mains supply is very much less than L, it has been ignored.

For the purpose of design and testing the current loop, the values of L, t_d and I_{Tol} were chosen as follows:

- To minimise the distortion at the zero crossing the value for L chosen was 10 mH.
- To achieve reasonable switching frequencies the tolerance band was initially chosen as ±0.1 A; that is, I_{Tol} =0.2 A.
- A reasonable value for the total implementation delay t_d which included blanking time, gate drive delay and control circuit was chosen as 10 μs

SIMULINK® model is used to simulate unipolar switching**.** This exercise was necessary to ensure that the transient and the steady state behaviour of the current loop were acceptable before the addition of the DC offset current control loop.

4. CCL SIMULATION

In unipolar switching, the operational behaviour of the current loop can be described by the differential equation 1.

$$\frac{di_S}{dt} = \frac{\left(SV_C - \hat{V}_S \sin\theta\right)}{L} \qquad (1)$$

As the inverter is to be used only in the converter mode, its rectifying configuration is ignored. The variable S, which describes the switching functions, is used to develop the SIMULINK model of the CCL circuit is shown in figure in 2 and are as follows: -

S = 1 if T_{A+} and T_{B-} are on
S = -1 if T_{A-} and T_{B+} are on

S = 0 if T_{A+} and D_{B+} are on *or* if D_{A+} and T_{B+} are on; alternatively
S = 0 if D_{A-} and T_{B-} are on *or* if T_{A-} and D_{B-} are on.

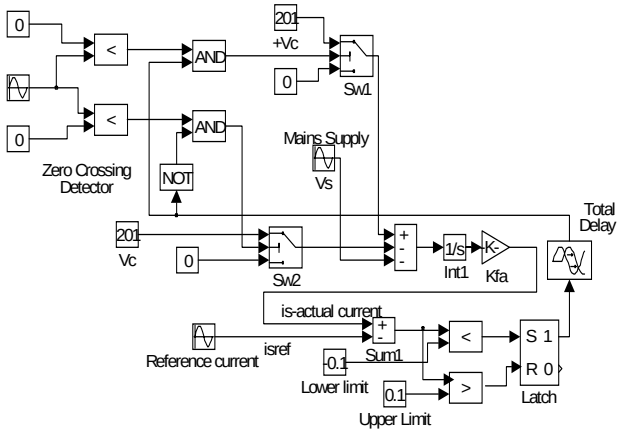

Figure 2: SIMULINK Model of Current Loop

For convenience, all the delays have been lumped together. Simulation results of the inverter output current using the parameters given in section 3 is shown in figure 3.

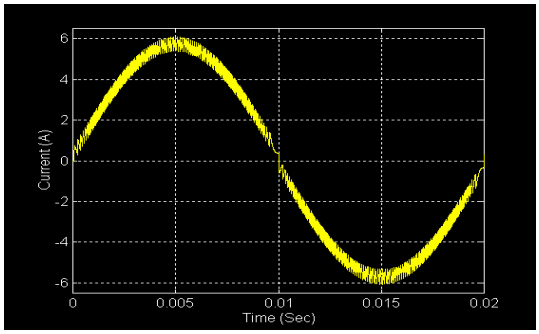

Figure 3: Inverter Output current I_s

The theoretical results obtained for the inverter system being proposed displayed no adverse dynamic characteristics at starting or during sudden changes in I_s. These favourable theoretical results allowed the design and construction of a 1 kW PV inverter system to proceed.

5. EXPERIMENTAL RESULTS WITHOUT DC CURRENT CONTROL

The aim of this subsection is two fold, firstly to validate the simulation results and secondly to identify the main source of DC offset current and hence justifying the need for a DC offset current control loop. A unipolar inverter using the current loop parameters from the theoretical analysis was then constructed.

Figure 4 shows the inverter output current when supplying about 500 W of power to the grid system.

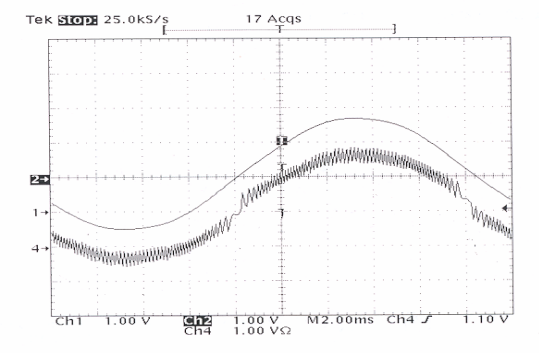

Figure 4: Inverter Output Current I_s

The steady state DC offset current component of the output current I_s varied between 12 mA and 34 mA when the power supplied by the inverter was varied. The DC offset current of 34 mA exceeded the maximum level, in this case of 21mA, specified by the Australian standards. Measurement of DC offset current revealed that the Hall Effect current sensor was main contributor of the DC offset current. However, while correcting the DC error introduced by the current sensor may solve problem this option was considered not suitable.

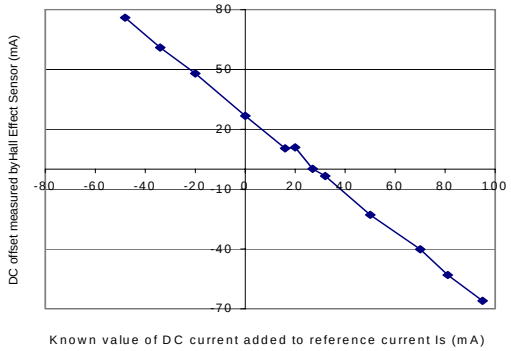

Figure 5: DC Current Present in Hall Effect Output

Figure 5 shows the result of adding known values of DC current to the reference signal and measuring the actual values of DC current present in the inverter output. This exercise shows that when 27mA of DC was added to the reference current, the Hall Effect sensor output indicated 0.2mA and when 0 DC offset current was applied to the reference current, the sensor output was 26.8mA. These results demonstrate the need to directly control the DC current present in the inverter output if the actual DC current injected into the grid is to remain within the legal limit.

6. DC OFFSET CURRENT REMOVAL

With reference to figure 6, it was envisaged that with the addition of a small voltage transformer (VT) and a PI controller instead of an integrator, the AC ripple voltage problems can be eliminated. Theoretically if the turns ratio of the VT was exactly 1:1 and is connected using correct polarity configuration, zero AC voltage would appear at the capacitor terminal in the DC offset control loop. The use of the PI controller was to ensure that the steady state error in the DC offset current was maintained at zero.

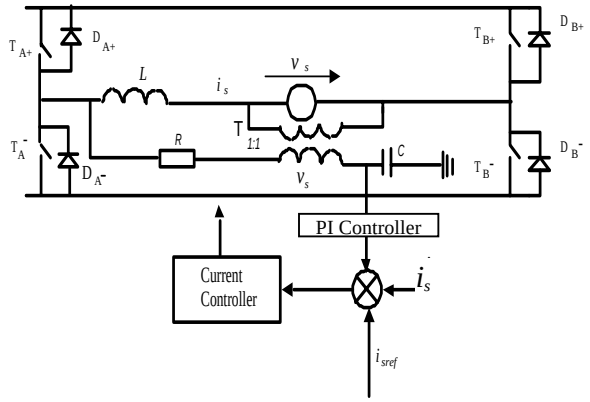

Figure 6: DC Offset Current Control Loop

7. SIMULATION RESULTS WITH DC OFFSET CURRENT CONTROL

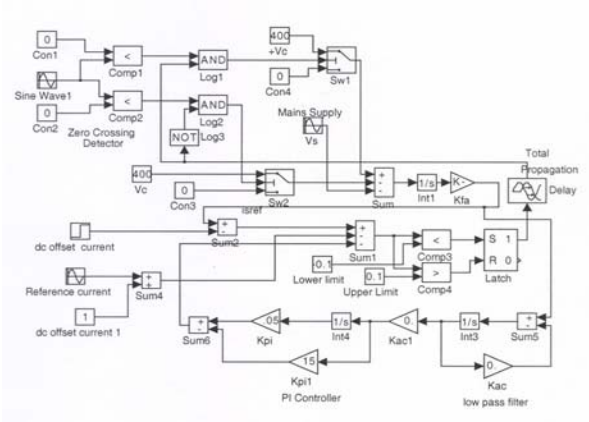

Figure 7: Simulink Model of Current Loop with DC Current Removal loop

The complete CCL shown in figure 7 was used to determine if the inclusion of the DC offset current control loop gave rise to any stability problems. A step increase of 2 A DC offset current was applied 0.05 seconds after the inverter system was turned on. The responses of the IP-controller and the current controller are shown in Figures 8 and 9. With the absences of any stability problems, when the CCL was subjected to such extreme variation in DC offset current allowed the experimental tests to proceed.

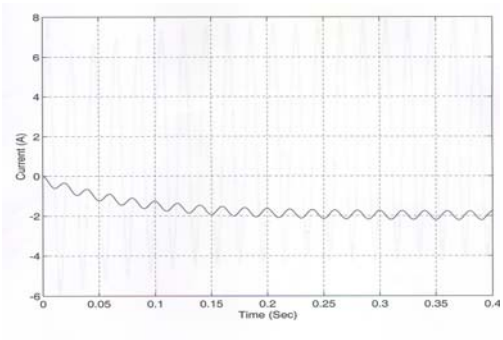

Figure 8: PI Controller Output

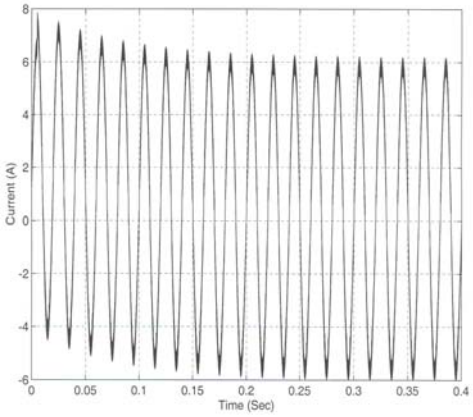

Figure 9: Inverter Output Current

8. EXPERIMENTAL RESULTS

The complete CCL with the DC offset current controller was designed and constructed. The inverter output current was varied and the DC component injected into the grid system from the inverter output was measured. Experimental results showed that the DC offset current remained at zero when the inverter power was increased from 0 to 500 W. When the DC controller was disabled and the inverter tested under the same load conditions, it was found that the DC offset current injected into the grid system varied between 16 mA and 28 mA. The inverter was test several times with and without the DC controller and in all cases total removal of the DC offset current was achieved.

The additional component cost for the DC offset current controller was less than $30. The cost of a power transformer and the additional solar panel capacity at about $6/W that would have been required to overcome its power losses was at least 10 times greater than the cost of the DC offset current controller.

9. CONCLUSION

A new technique to remove the DC offset current from the output of a unipolar, current control, transformerless PV inverter for utility connection has been realised. Experimental results presented confirm that zero DC offset current can be maintained irrespective of its source. The proposed DC current control method is cost effective, does not have any adverse effect on the dynamic response of the current controller. The removal of the DC current has been achieved without sacrificing the overall conversion efficiency of the inverter system. This DC control technique can also be used in bipolar switched inverters and in inverter applications where transformers are used to improve the quality of power fed to the grid network.

10. ACKNOWLEDGEMENT

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