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ABSTRACT

Synchronous detection is used to detect and measure very low-level signals in the presence of significant noise. A defining characteristic of this measurement approach is the use of a periodic probe signal to excite the system under test. This is followed by mixing of the reference signal and its phase-quadrature with the measured signal. Standard analog to digital converters are employed, usually with the mixing and filtering performed digitally. Most practical high-resolution analog to digital converters employ oversampled sigma-delta modulation and are incorporated as a separate functional block. This paper derives a processing algorithm that combines the oversampled analog to digital conversion with signal mixing into one functional block. There are several important advantages of this approach. The computational complexity of the lock-in amplifier is substantially reduced, with no loss of accuracy. Moreover, the requirement for high-resolution analog-to-digital conversion is relaxed; it is replaced with low-resolution high-rate sampling, which is typically much easier to realize in practice. Experimental results are presented to demonstrate the correctness of the technique as determined via theory and simulation.

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I. INTRODUCTION

The measurement of very low-level signals is a common problem in physical instrumentation and measurement systems. In a specific case where the system under test can be excited by a known sinusoidal input, the application of the synchronous demodulation technique enables accurate measurements to be performed at exceedingly low signal-to-noise ratios. The basic positioning of a lock-in amplifier is illustrated in Fig. 1. The signal source is applied to the measurement system, with a phase-quadrature signal available or synthesized using phase-lock techniques. The result is the gain $\widehat{A}$ and phase $\widehat{\varphi}$ estimates of the system under test.

The performance limits of the lock-in amplifier (LIA) have received research attention for some time.[1] More recently, programmable hardware has been employed,[2] and other novel techniques to improve resolution have been put forward.[3] There continues to be interest in the lock-in measurement technique, both from a general signal processing and measurement perspective and when the approach is tailored to particular scientific measurement scenarios such as nonlinear intermodulation[4] and multiple simultaneous measurements.[5]

A number of implementations, refinements, and extensions have been put forward in the literature, with the lock-in functionality tailored to specific applications. These include operation at high frequencies,[6] applications in spectroscopy,[7] precise timekeeping,[3] and industrial chemical species tomography.[8] The usefulness of the concept has led to its adoption beyond the laboratory, for example, in maximum power point tracking (MPPT) for solar arrays,[9] power inverter harmonic compensation,[10] and motor fault signature detection.[11] Depending on the context, these applications have signal-to-noise requirements down to −40 dB.

With these observations in mind, we seek a simpler yet functional alternative. It is evident that the nature of the A/D conversion can be incorporated into the synchronous detection using the feedback inherent in oversampling A/D converters. This constitutes the new approach presented in this paper, with the design detail derived and experimental evaluation presented to validate the algorithm.

A/D converters may be created using one of several different approaches, each with complexity, speed, and resolution tradeoffs. Due to the reduced requirements for precision components and calibration, oversampling converters are generally favored in practice. The dominant approach in A/D conversion is ΣΔ modulation. In this method, a simple (usually one-bit) quantizer is used in a feedback configuration, with exceedingly high sample rates. This enables lower cost and easier fabrication. The ΣΔ converter is able to perform noise shaping, whereby quantization noise is moved

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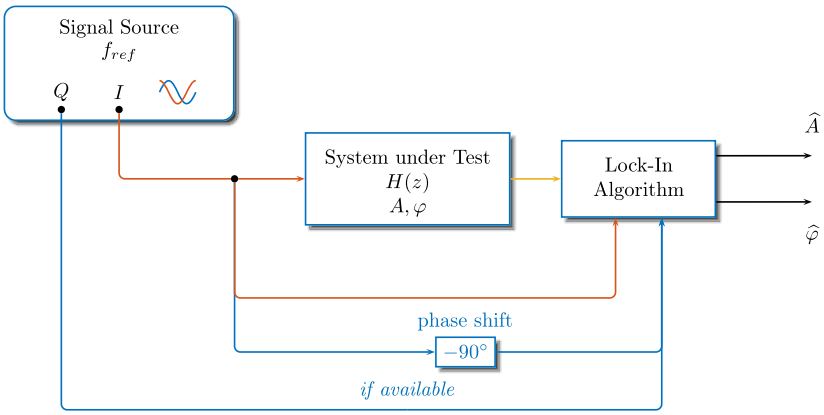

FIG. 1. Location of the lock-in amplifier in a measurement system. The system under test is excited by a sinusoidal input. The source oscillator produces a quadrature-phase waveform (or it may be synthesized via a phase delay). These reference signals, together with the sampled system output, become inputs to the algorithm that estimates the gain $\widehat{A}$ and phase shift $\widehat{\varphi}$. This fully characterizes the unknown system at the input frequency.

to a band outside the band of interest. Extensive theoretical treatment of ΣΔ modulation[12] informs the design of such systems in practice. The noise power resulting from ΣΔ modulation, which is particularly relevant in a measurement context, has been extensively analyzed.[13] Extension of lowpass ΣΔ to bandpass operation (as would be required for a lock-in amplifier) via pole-zero placement requires special care with pole placement for stability.[14]

The LIA may be operated with a square-wave reference. However, this depends on the measurement quantity, and typically, many types of optical, acoustic, or other transducers require a sinusoidal excitation. In addition, odd harmonics using a square reference require special treatment.[15,16]

The use of conventional A/D conversion with an LIA means that the sampled data are treated as a B-bit number, where typically $B > 12$ for instrumentation applications. However, since oversampling ΣΔ modulator produces a single-bit stream, it is logical to investigate whether LIA processing can be performed directly on this bistream; this has been done for the detection of impulsive noise.[17]

Calculation of correlation directly in the ΣΔ domain has been suggested,[18] but this has not been extended to the functionality required for physical measurements of gain and phase in a measurement context. It has also been demonstrated that certain adaptive digital signal processing (DSP) algorithms could be directly implemented using oversampled ΣΔ modulation.[19]

Another important functional block required by the LIA is an oscillator, for generating excitation for the system under test. A common approach to variable frequency generation is direct digital synthesis (DDS). DDS has been extended to incorporate ΣΔ modulation rather than a separate D/A converter.[20] Single-bit D/A conversion was found to produce higher dynamic range (DR) and better spur-free dynamic range (SFDR).

II. OUTLINE OF THE PROPOSED DESIGN

The proposed design approach incorporates the key advantages of ΣΔ converters and performs the function of a lock-in amplifier for low signal-to-noise ratio (SNR) measurements. The design has the following advantages:

1. No precision D/A converter is required, eliminating a possible source of nonlinearity.
2. Fast A/D conversion is performed, with no precision component tolerance issues.
3. No floating-point multiplications are required for each sample acquired.

The first two of these are shared with ΣΔ converters. Since a conventional LIA requires one A/D converter and usually one D/A converter, the complexity is somewhat reduced. Furthermore, the mixing operation in the digital domain requires two multiplications to be performed for each sample acquired, one for the reference and another for the phase quadrature of the reference. These operations are eliminated in the proposed design and incorporated into the lowpass filter itself. There is optionally, one scaling multiplication for the final measurement, if calibration of amplitude is required. This is not needed in measurement scenarios where ratiometric or relative amplitudes are measured. This single multiplication, if required, is substantially less than two multiplications per sample needed in a conventional LIA employing multibit A/D and D/A converters.

III. PROPOSED APPROACH

In the present contribution, we employ ΣΔ modulation as an integral part of the LIA. Thus, it is appropriate to briefly review the research context pertaining to these approaches. Since waveform generation is also required for the LIA, we also mention the commonly used DDS technique. Our proposed approach dispenses with the additional complexity of a DDS block within the LIA.

Synchronous demodulation may be broken down into the following functional blocks: frequency synthesis for the excitation, sampling of an analog signal using one of several possible A/D topologies, multiplication of reference and measured signals, and lowpass filtering. The basic architecture (Fig. 2) is well known. The key contribution of this paper is to combine the A/D converter blocks, the multiplication, and lowpass filtering into one algorithm operating in the switched-sample domain using oversampling. Extension of the original concept[21] presented here includes a more thorough analytical treatment required for precise measurements and experimental results to demonstrate effectiveness.

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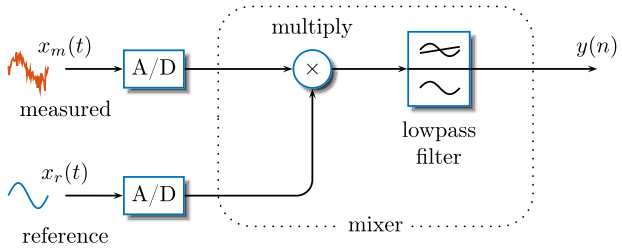

FIG. 2. One channel of a synchronous detector. Usually, quadrature channels are employed. The reference may be generated internally (requiring a D/A converter) or sampled as depicted (using an A/D converter).

IV. DERIVATION

The proposed approach embodies oversampling and lowpass filtering. For completeness, it is useful to present a brief review of oversampled A/D converters incorporating the ΣΔ approach before expanding on the proposed LIA design.

A. ΣΔ conversion

Extending the idea of oversampling, the ΣΔ has become the dominant method of A/D conversion, due to substantially reduced tolerance requirements for both A/D and D/A subsystems. The quantization is performed using a simple quantizer (usually one-bit) in a feedback loop configuration as illustrated in Fig. 3.

The basic feedback loop arrangement may be applied to both A/D and D/A subsystems. The accumulated error $s(n)$ between the input signal $x(n)$ and the discrete representation $d(n)$ is forced to zero as a result of the feedback loop. In this way, a large number of one-bit samples takes the place of a single, more accurate, conversion word. Naturally, this requires a lowpass filtering operation as depicted.

For the LIA system, at least one ΣΔ modulator is required for sampling the unknown measured signal. The reference may be sampled, in which case, a second ΣΔ is needed. Alternatively, the reference may be generated from within the measurement subsystem, in which case, the ΣΔ modulator is configured as an oversampled signal source.

B. Synchronous detection

In the LIA, the unknown signal $y_m(n)$ is measured, and depending on the situation, the reference $y_r(n)$ is either measured

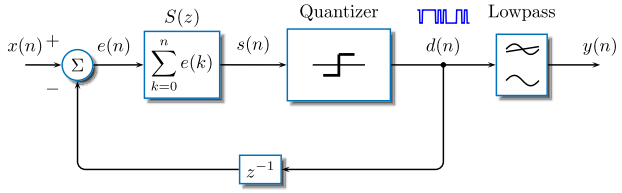

FIG. 3. The fundamental ΣΔ loop concept (after Ref. 22). A large number of low-resolution samples are taken to effect a higher-resolution measurement.

(if generated externally) or generated internally (hence, immediately available for computation). This is then followed by multiplication and lowpass filtering. Let the product of the measured and reference at n be

$$p_{mr}(n) = y_m(n) \cdot y_r(n), \tag{1}$$

where subscript m denotes the measured quantity and r denotes the reference.

The ΣΔ component of a conventional A/D can be merged with the LIA computation. Let $d(n)$ be the ΣΔ output samples. The LIA product of measurement y_m and reference y_r is then of the form,

$$\begin{aligned} p_{mr}^{(P)}(n) &= y_m(n) \cdot y_r(n) \\ &= [d_m(n) + d_m(n-1) + \cdots + d_m(n-P+1)] \\ &\quad \cdot [d_r(n) + d_r(n-1) + \cdots + d_r(n-P+1)]. \end{aligned} \tag{2}$$

A standard approach to reduce such a long finite impulse response (FIR) filter is to reduce it to a recursive one. Using a conventional cascaded integrator-comb recursive formulation for each filter separately, this can be written recursively as

$$\begin{aligned} p_{mr}^{(P)}(n) &= y_m(n) \cdot y_r(n) \\ &= [\, y_m(n-1) + d_m(n) - d_m(n-P)] \\ &\quad \cdot [\, y_r(n-1) + d_r(n) - d_r(n-P)]. \end{aligned} \tag{3}$$

For single-bit conversion, $d(n) \in [-1, 1]$, and so products such as $d(n)y(n)$ can be computed without multiplication; however, products of the form $y(n)y(k)$ still require multiplication. Thus, even if the oversampled stream is available, using that in conjunction with the lowpass filtered oversampled stream still requires at least one multiplication for each of the in-phase and quadrature-phase branches of the LIA.

Careful re-ordering of the functional blocks permits this limitation to be overcome. Returning to the direct nonrecursive form, we may rewrite and expand the filtered product, averaged over P samples, as

$$\begin{aligned} p_{mr}^{(P)}(n) &= [d_m(n) + d_m(n-1) + \cdots + d_m(n-P+1)] \\ &\quad \cdot [d_r(n) + d_r(n-1) + \cdots + d_r(n-P+1)] \\ &= d_m(n) \sum_{k=0}^{P-1} d_r(n-k) + d_m(n-1) \sum_{k=0}^{P-1} d_r(n-k) \\ &\quad + \cdots + d_m(n-P+1) \sum_{k=0}^{P-1} d_r(n-k). \end{aligned} \tag{4}$$

The previous filtered product averaged over P samples is

$$\begin{aligned} p_{mr}^{(P)}(n-1) &= [d_m(n-1) + d_m(n-2) + \cdots + d_m(n-P)] \\ &\quad \cdot [d_r(n-1) + d_r(n-2) + \cdots + d_r(n-P)] \\ &= d_m(n-1) \sum_{k=1}^{P} d_r(n-k) + d_m(n-2) \sum_{k=1}^{P} d_r(n-k) \\ &\quad + \cdots + d_m(n-P) \sum_{k=1}^{P} d_r(n-k). \end{aligned} \tag{5}$$

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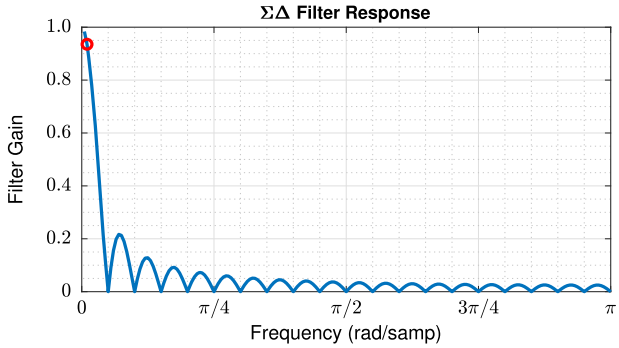

FIG. 4. The sinc response of the oversampling filter is illustrated here. The operating point is shown with a red circle. This corresponds to the excitation frequency and shows the gain introduced by the algorithm at that specific frequency. This gain acts as a multiplier for the computed gain, and the actual system gain is found by dividing the computed gain by this amount.

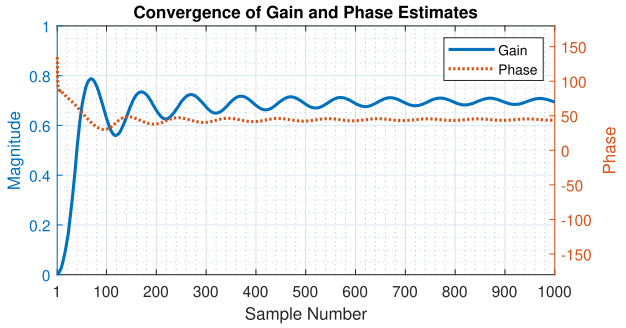

FIG. 6. Convergence of the simulated ΣΔ LIA when no noise is present. The measured gain is shown without taking the final scaling into account. The initial estimates, when few samples are available for averaging, are poor. In particular, the phase requires an arctangent computation that can be far from the final value. Nevertheless, the convergence of both gain and phase is evident with an increasing number of samples.

For the convenience of notation, we define the P-term summation starting at a given index n or $(n-1)$ as

$$\sum_P s(n) \triangleq s(n) + s(n-1) + s(n-2) + \cdots + s(n-P+1)$$
$$\sum_P s(n-1) \triangleq s(n-1) + s(n-2) + s(n-3) + \cdots + s(n-P). \quad (6)$$

Subtracting the equations for $p_{mr}(\cdot)$, expanding, and canceling terms, we obtain a recursive result for computing $p(n)$,

$$p_{mr}^{(P)}(n) = p_{mr}(n-1) + \left[d_m(n) \sum_P d_r(n) + d_r(n) \sum_P d_m(n) - d_m(n) d_r(n) \right] - \left[d_r(n-P) \sum_P d_m(n-1) + d_m(n-P) \sum_P d_r(n-1) - d_m(n-P) d_r(n-P) \right]. \quad (7)$$

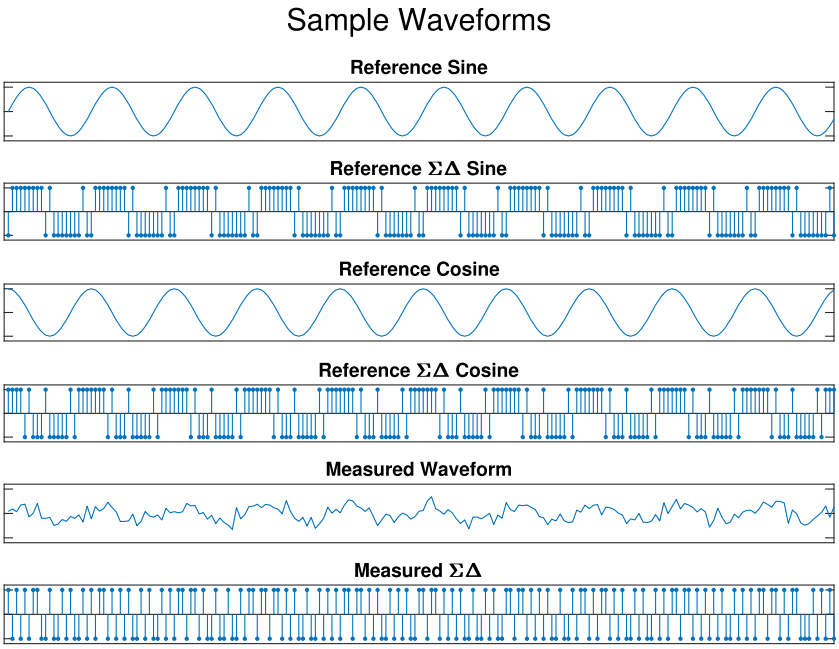

FIG. 5. Sample waveforms for numerical simulation. The reference waveforms are generated using ΣΔ techniques, and the measured waveform from the transducer or device under test is sampled using the ΣΔ method.

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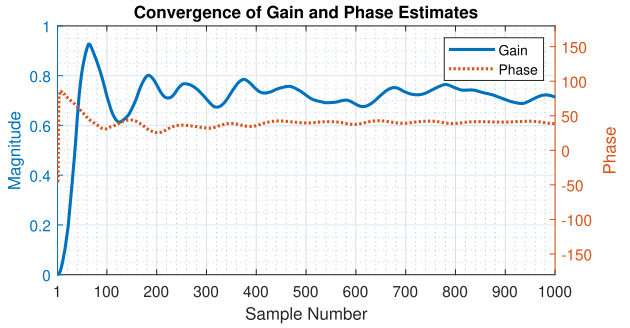

FIG. 7. Convergence of the simulated ΣΔ LIA, with noise present. The SNR is −10 dB. The initial estimates are of low accuracy, but even with this significant amount of noise, the convergence to final values is evident.

TABLE I. Simulation results for a system chosen to have $A = 0.2$, $\varphi = -60°$. The algorithm parameters are $N = 1000$ samples in total, $M = 200$ points per cycle, and filter order $P = 40$.

SNR (dB)	A	φ (deg)	$\widehat{A}$	$\widehat{\varphi}$ (deg)
∞	0.2	−60	0.19	−59.6
10	0.2	−60	0.19	−59.3
3	0.2	−60	0.19	−59.7
0	0.2	−60	0.19	−61.3
−3	0.2	−60	0.18	−55.6
−10	0.2	−60	0.18	−64.5

Again, $d(n) \in [-1, 1]\ \forall n$, and thus, it is evident that no multiplication is required, and only accumulation and sign changes. This means that the LIA computations can be performed directly in the ΣΔ oversampled domain, provided (7) is adhered to.

The FIR-filtering inherent in (2) results in a sinc response in the frequency domain. Because both the reference and measured signals pass through these identical filters and are then multiplied, the effective gain depends on the sinc-squared response. The phase, however, does not require a similar adjustment. This is because both signal paths pass through identical filters, with identical phase shifts. To compensate for the gain of the sinc filters, with an order P filter, the operating point is

$$H(z) = \frac{1 - z^{-P}}{1 - z^{-1}}, \tag{8}$$

$$= \frac{z^P - 1}{z^{P-1}(z - 1)}. \tag{9}$$

For a fixed reference frequency at M samples per cycle, $z = \exp(\jmath\omega_{ref}) = \exp(\jmath 2\pi/M)$, and thus,

$$H(z)|_{z=\exp(\jmath\omega_r)} = \frac{1 - \exp(-\jmath 2\pi P/M)}{1 - \exp(-\jmath 2\pi/M)}. \tag{10}$$

The required gain adjustment is thus the reciprocal of this. Taking into account the filter length, this gain G_s becomes

$$G_s = P \cdot \left| \frac{1 - \exp(-\jmath 2\pi/M)}{1 - \exp(-\jmath 2\pi P/M)} \right|. \tag{11}$$

This gain adjustment must be applied twice, as explained above. This is illustrated in Fig. 4, where the operating point depends on P and M. Typically, this is very close to, but not equal to, unity. This final compensation is only required once per measurement cycle, not on each sample taken.

V. RESULTS

In the following sections, an implementation using simulated data to thoroughly check and verify the correct operation is provided. Then, the operation of the method on a resource-constrained microcontroller is demonstrated, showing that the gain and phase of a simple one-pole lowpass filter circuit can be measured successfully. Taken together, the simulation and experimental approaches provide evidence that the proposed technique is both technically correct and practically feasible.

VI. NUMERICAL VERIFICATION

Figure 5 shows the waveforms with the reference excitations (I and Q) generated with the ΣΔ approach. The system output is corrupted by noise and is sampled using the ΣΔ method.

Applying (7) to the ΣΔ domain waveforms, we find the convergence to the unknown system parameters as shown in Fig. 6 for the noise-free case. Here, $N = 1000$ samples are acquired for the entire

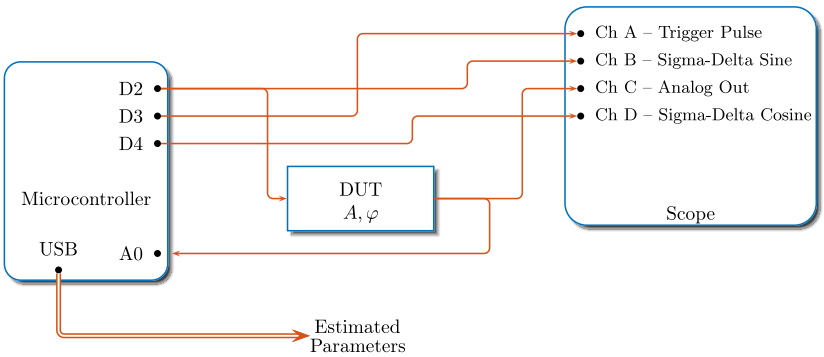

FIG. 8. Block diagram of the experimental setup for proof-of-principle that lock-in measurements can be performed using ΣΔ oversampling.

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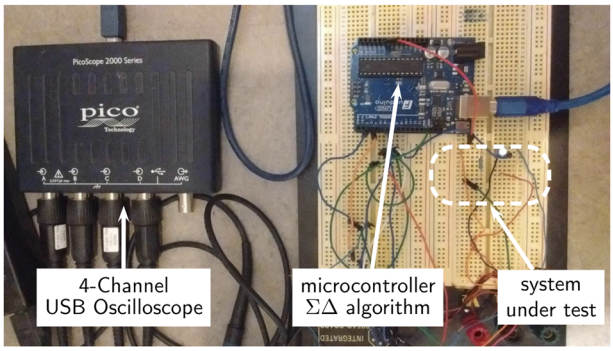

FIG. 9. The actual experimental setup employed for the proof-of-principle evaluation.

measurement interval, with $M = 200$ samples per reference cycle, and a filter order of $P = 40$. The theoretical values of amplitude and phase are $A = 0.8, \varphi = +45°$, and the resulting estimated parameters (after sinc correction) are $\widehat{A} = 0.79$, $\widehat{\varphi} = +43.6°$.

Figure 7 is shown for the same case of $N = 1000, M = 200$, $P = 40$ but with additive white Gaussian noise (AWGN) such that the SNR is −10 dB. This represents a more demanding case for lock-in detection. Estimated parameters are $\widehat{A} = 0.81$, $\widehat{\varphi} = +38.6°$. Table I summarizes a number of representative cases at various SNR values.

VII. EXPERIMENTAL VERIFICATION

The numerical simulations shown have established the correctness of the proposed approach. It is imperative to test the proposal using real hardware; the testing is described in this section. A block diagram of the setup used for testing is shown in Fig. 8. A picture of the realized experimental setup is shown in Fig. 9.

The algorithm was tested using a resource-constrained microcontroller as follows: A simple one-pole lowpass filter was constructed, being representative of the simplest type of transfer function envisaged. The results reported are designed to demonstrate the correctness of the approach in measuring both gain and phase; they do not purport to convey or explore every possible parameter variation such as the filter length.

The microcontroller used for this demonstration is an ATMEL AT328P 8-bit microcontroller. This RISC device has a limited memory for both program data and variables, as well as a relatively low 16 MHz clock rate.

The ΣΔ analog to digital sampling was performed using the microcontroller A/D, with a ΣΔ loop as described. The code is shown in Fig. 10. In this code section, the on-chip sampling register ADCH

```
// A/D read, feeds into SDM

x = (long)ADCH;
x -= Amax;

// find current error, accumulate
eAD = x - sumAD;
esumAD += eAD;

// A/D value switches on error +/-
dAD = eAD > 0 :1:-1;

// integrate A/D final value
sumAD += dAD;
```

FIG. 10. Analog to digital code for ΣΔ modulation loop. Comparing with Fig. 3 for the analog to digital case, the variable `x` represents the sample $x(n)$, `eAD` is the error $e(n)$, `esumAD` is the integration $s(n)$, and `dAD` is the single-bit quantized value $d(n)$.

```
// D/A
// xi,xq scaled sine and cosine refs

// calculate error, accumulate sum
eDA = xi - dDA*Amax;
esumDA += eDA;

// switch output according to
// accumulated error
dDA = esumDA > 0 ? 1:-1;

// write digital output
// digital out pin, port D pin 2, high
if( dDA > 0 )
  PORTD |= (1 << DDD2);
else
  PORTD &= ~(1 << DDD2);

// quadrature channel
eDAq = xiq - dDAq*Amax;
esumDAq += eDAq;

// switch output according to
// accumulated error
dDAq = esumDAq > 0 ? 1:-1;
```

FIG. 11. The digital to analog code for the ΣΔ modulation loop. Comparing with Fig. 3 for the digital to analog case, the variable `xi` represents the pre-stored lookup table for a particular sinusoidal point in the waveform, `dDA` is the switched output signal $d(n)$, and `esumDA` is the error integration $s(n)$. These variables are mirrored for the quadrature-signal case with `q` appended.

```
// Update products for oversampled data
for(i = 0; i < P; i++ )
{
    dsumDA  += dBufDA[i];
    dsumDAq += dBufDAq[i];
    dsumAD  += dBufAD[i];
}

psum += dsumDA*dsumAD;
```

FIG. 12. Filtering and multiplication section for the lock-in component. Here, the output of the summation block of Fig. 3 is computed, for each of the in-phase sine, the quadrature-phase sine, and the oversampled analog-to-digital conversion. The product term may be directly computed using multiplication or more simply with the recursive computation developed in Eq. (7).

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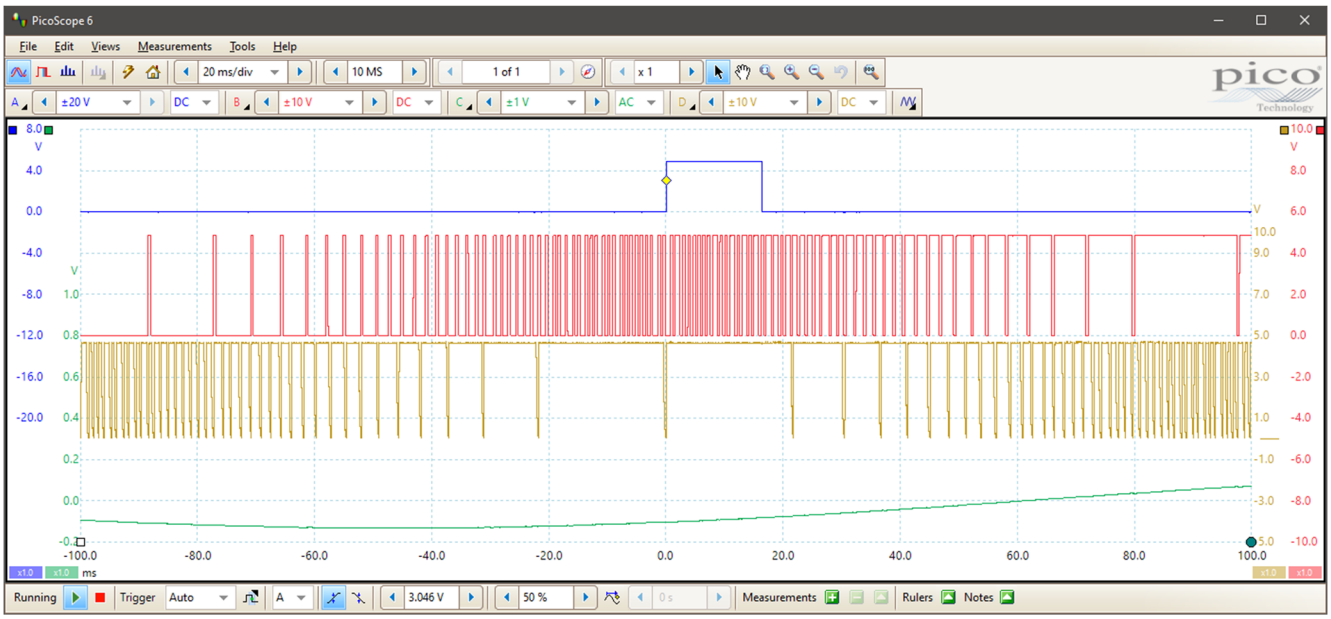

FIG. 13. Actual measured waveforms for the microcontroller implementation, showing details of the synthesis of the switched signal (blue = sync pulse, red = in-phase, brown = quadrature-phase, and green = analog waveform). Shown are the ΣΔ waveforms for I and Q references. The upper pulse is for display timing synchronization only. The timebase is 20 ms/div.

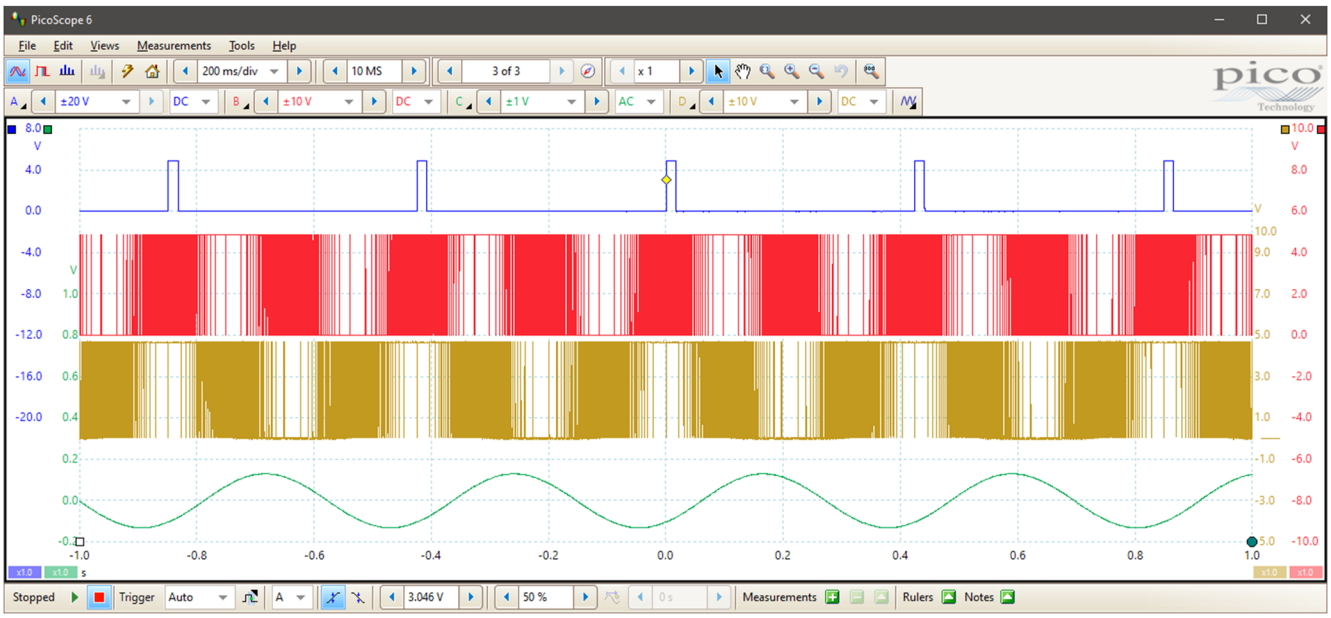

FIG. 14. Actual measured waveforms for the microcontroller implementation, showing several reference cycles (blue = sync pulse, red = in-phase, brown = quadrature-phase, and green = analog waveform). The ΣΔ waveforms for I and Q references are shown, together with the output from the lowpass filter under test. The upper pulse is for display timing synchronization only. The timebase is 200 ms/div.

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TABLE II. The results for embedded LIA testing of a first-order RC lowpass filter with $R = 68\ \Omega$. The parameters in this test are filter length $P = 40$, samples per cycle $M = 200$, sample rate 500 Hz, and scale constant (per channel) 1.068 915.

	Gain		Phase	
C (μF)	ΣΔ-LIA	Theory	ΣΔ-LIA	Theory
0.47	0.98	0.96	−16.8	−17.0
1	0.80	0.82	−37.0	−36.3
10	0.14	0.14	−81.1	−82.1

is read and scaled accordingly. The error is then computed and accumulated. This corresponds to the subtraction and summation stages shown in Fig. 3. The single-bit digital output `dAD` is then determined by the sign of the error value and is also accumulated.

The digital to analog conversion, required for exciting the system under test, also uses ΣΔ principles. The core code for this is shown in Fig. 11. Here, the error term `eDA` is calculated as the difference between the reference sine (or cosine) and the switched amplitude `dDA * AMax`. This value is then integrated and compared with a threshold of zero. This then forms the next switched digital output `dDA`. A similar approach is followed with the quadrature channel computations, with "q" in the variable names denoting the quadrature channel.

The proposed algorithm incorporates the filtering aspect of a conventional ΣΔ ADC, with the signal mixing required for lock-in functionality. This is shown in Fig. 12, where a direct computation is shown for what may be recursively computed using Eq. (7).

The measured waveforms are illustrated in Figs. 13 and 14. The fine structure of the ΣΔ switching waveform, and the analog approximation over several cycles, are evident.

The results from a number of one-pole lowpass filter parameters tested are summarized in Table II. It is evident that the approach successfully performs the function of a lock-in amplifier but using the ΣΔ approach.

From the outline presented, it is evident that implementation of an FPGA is also feasible, using only a limited subset of resources. In fact, since ΣΔ conversion requires only digital operations, it is eminently suited to devices with no analog capability.

VIII. DISCUSSION

It has been shown that the proposed approach yields equivalent measurement results when the inherent nature of the system is lowpass in the frequency domain. The many advantages that have seen ΣΔ conversion replace alternative analog-to-digital conversion approaches in many other applications are directly transferrable to the precision measurement context. In fact, the incorporation of a loop filter provides other design advantages for noise shaping. Advantages in the scientific measurement context include the fact that no digital-to-analog converter is required; no analog-to-digital converters are required, and furthermore, if an A/D converter is available, then its precision (number of bits) may be increased arbitrarily, subject to the limitation of processing speed. In the method described here, direct hardware implementation (via FPGA) is made substantially easier, and there is no floating-point multiplication required per sample.

IX. CONCLUSION

This paper has presented an approach to the lock-in amplifier method for synchronous detection using two-valued signals and the ΣΔ approach. Doing so greatly simplifies embedded applications and negates the need for separate A/D conversion stages. It was shown mathematically that the result is identical to multibit sampling with an FIR filter. Simulation results confirmed the validity of the algorithm, and experimental results using an embedded microcontroller conclusively show that the algorithm works in practice. This enables a greatly simplified design and implementation for continuous-time signal sensing and measurement.

AUTHOR DECLARATIONS

Conflict of Interest

The author has no conflicts to disclose.

Author Contributions

J. Leis: Conceptualization (equal); Investigation (equal); Methodology (equal); Resources (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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